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20 August 1986—31 December 1989

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16. Abstract (Limit 200 Words)

A 480 × 4 element charge imaging matrix (CIM) scanning focal plane has been developed for IR search/track applications in the 8- to 12-μm band. The CIM array consists of 8 rows of 240 elements on 3-mil centers (cross-scan), with an active pixel area of 1.6 × 1.7 mil^2, and four stages of time-delay-and-integration (TDI). Arrays are fabricated in thinned LWIR HgCdTe and vertically interconnected to underlying custom-designed Si IC processors. A linear (480 × 1) version of the design was also implemented, along with wire-bondable (nonvertically integrated) versions of both arrays for performance analysis and diagnostics. A parallel technology study addressed LWIR CIM performance issues, including detector noise mechanisms, diode leakage current and noise reduction, 1/f noise sources, and the effects of substrate thinning on p-type HgCdTe MIS properties.

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16. Abstract (Continued)

Bondable arrays of both configurations (linear and TDI) were completed and operated in single row-and-column mode at T = 65 to 80 K and 5×10^{15} background ($f/3$). Measured single-pixel responsivities were in the range of 6 to 12 MV/W (CIM output referred) at $\lambda_p = 9.8$ μm, dependent on integration time. Saturation signal flux exceeded $2 \times 10^{16}/cm^2s$ at all integration times, with excellent linearity. Detector sensitivity was dominated by excess test-system noise.

Custom Si processors for the vertically integrated (VICIM) configuration were designed, fabricated, and tested, and met or exceeded all design specifications. Results of the technology study demonstrated that p-type HgCdTe could be thinned to less than 10-μm substrate thickness with attendant enhancement of MIS properties, and that CIM diode leakage could be significantly reduced by postannealing of ion-implanted diodes. These results, together with the demonstrated bondable-array performance, comprise the necessary ingredients for further VICIM FPA development.

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SECTION I
INTRODUCTION

The development of LWIR HgCdTe charge imaging matrix (CIM) detector arrays has arisen from the requirement for high-efficiency, high-speed (approximately 2-MHz data rate) scanning IR focal planes operating in the 8- to 12-μm spectral band for airborne infrared search/track (IRST) and next-generation FLIR systems. Under the present contract, the contractor undertook design and development of a 480 × 4 scanning CIM array for IRST, designed to the specific requirements of the Navy's High-Altitude Remote Platform Sensor System (HARPSS). The program included a parallel technology study to address issues related to CIM noise performance and detector performance enhancement. Both efforts represent a continuation of previous programs with the Naval Research Laboratory to develop the 10-μm CIM detector technology.[1,2]

In the previous development effort under Contract N00014-84-C-2337, basic measurements of CIM responsivity, charge-transfer efficiency (CTE) at high data rates, linearity, crosstalk, blooming, and noise characteristics were completed. These initial results demonstrated that the CIM is capable of 2-MHz data rates with high CTE (>95 percent). The unique column-diode readout structure results in low sense-node capacitance and high detector responsivity (>3 × 10^6 V/W). Clocking schemes using near-100-percent duty cycles give good crosstalk characteristics, and the readout diode, which acts as a drain during charge integration, provides excellent resistance to blooming

In the present program, the advantages of the CIM approach were exploited in the design and fabrication of a 480 × 4 scanning array for IRST, shown in Figures 1-1 and 1-2. The array is configured as a 240 × 2 × 4, 1920-element matrix with oversampling in cross-scan, providing 480-element scan line with four stages of time-delay and-integration (TDI). Overall device length is 765 mils, with pixels arranged on 3-mil centers. Output signals are multiplexed and processed by a custom-designed silicon IC processor chip (Figure 1-3). Coupling of the detector array to the silicon IC is accomplished by means of vertical interconnections at each of the CIM output nodes (Figure 1-4). For development and diagnostic purposes, a linear (non-TDI) version of the design was also implemented, combining a pair of independent 480 × 1 arrays on a single CIM matrix of the same overall length. A completed example is shown in Figures 1-5 and 1-6. The linear CIMs could be bonded in conventional fashion to existing IC processors or vertically integrated with a custom-designed linear version of the TDI processor (Figure 1-7).

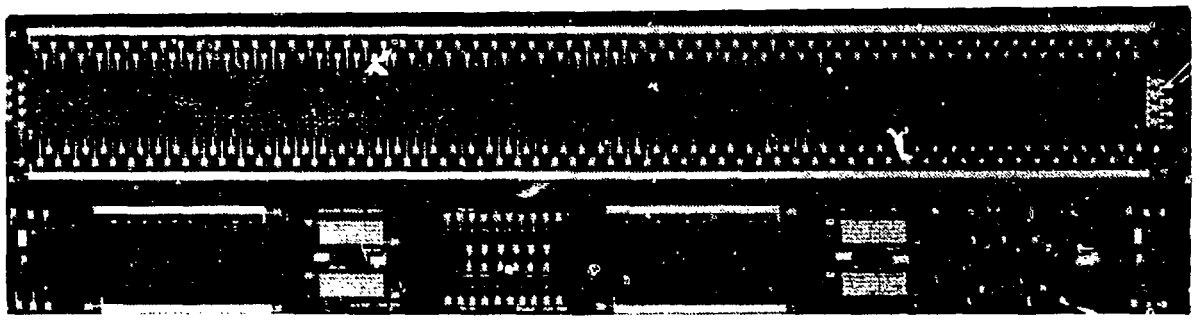


Figure 1-1. 480 × 4 TDI charge imaging matrix for IRST.

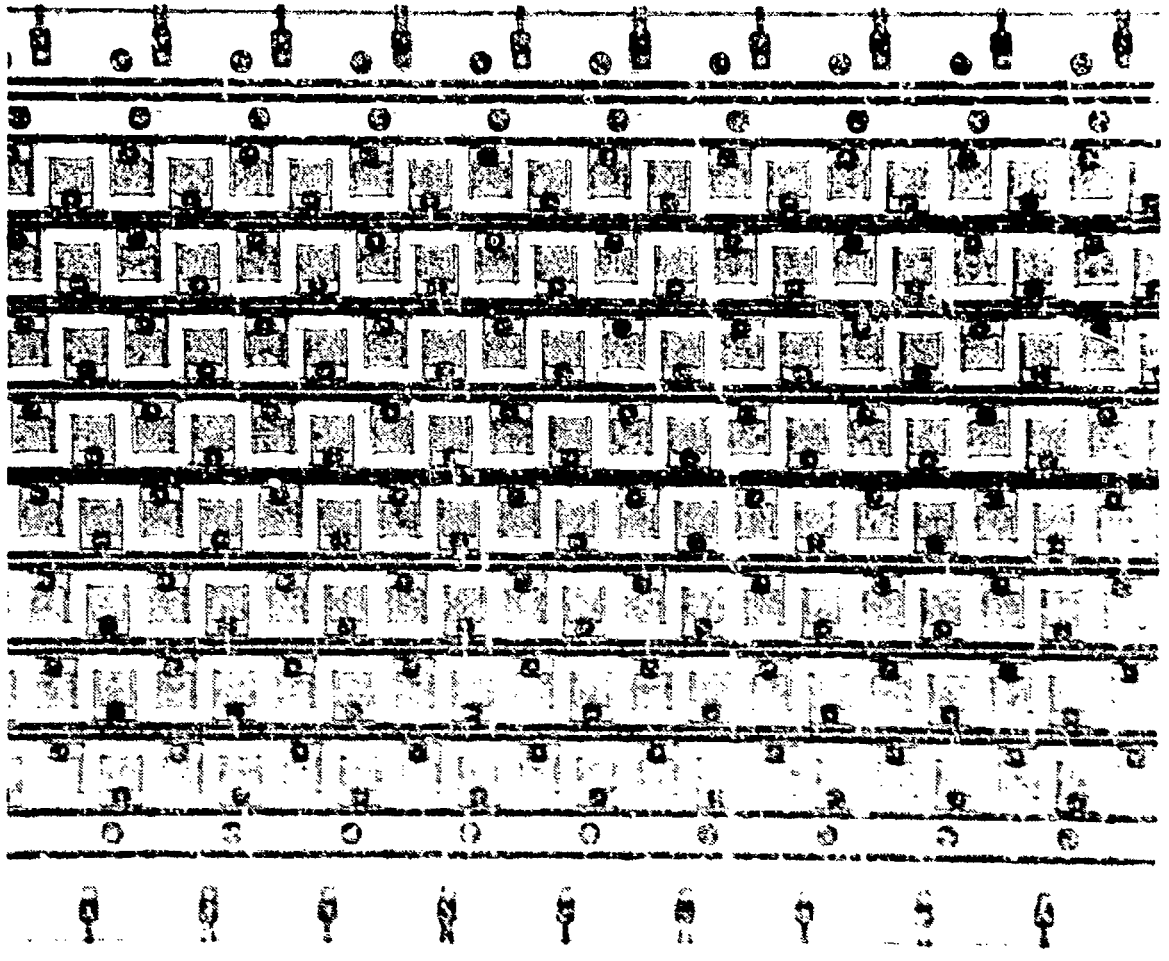


Figure 1-2. Detail of active area of 480 × 4 TDI CIM array.

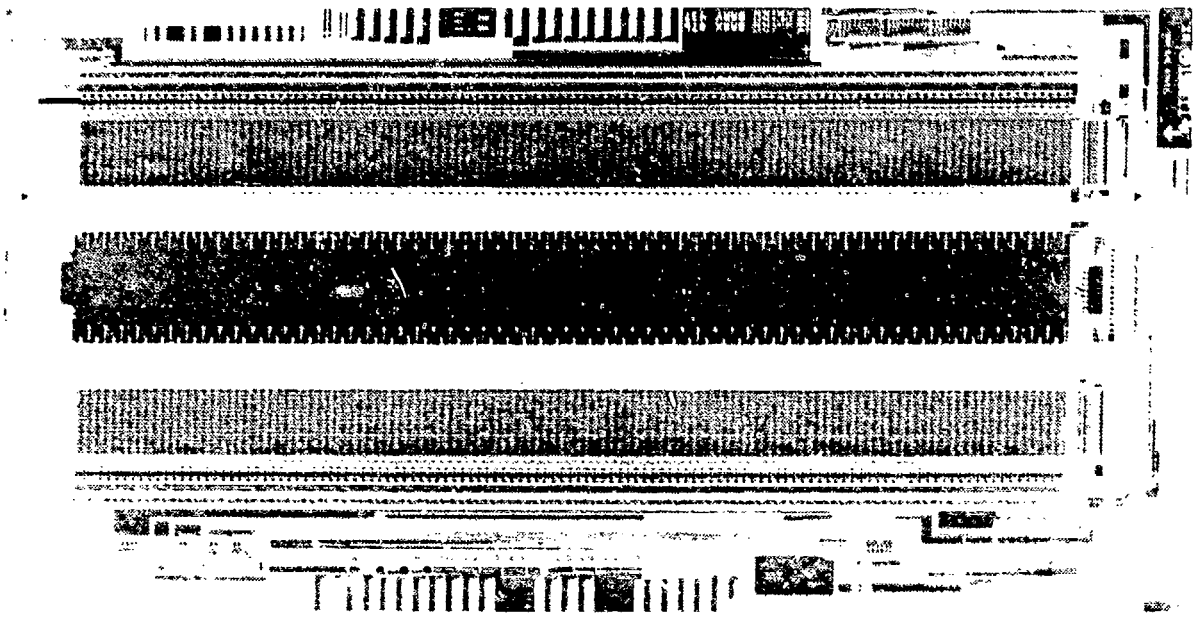


Figure 1-3. Custom-designed silicon IC processor for 480 × 4 IRST CIM array.

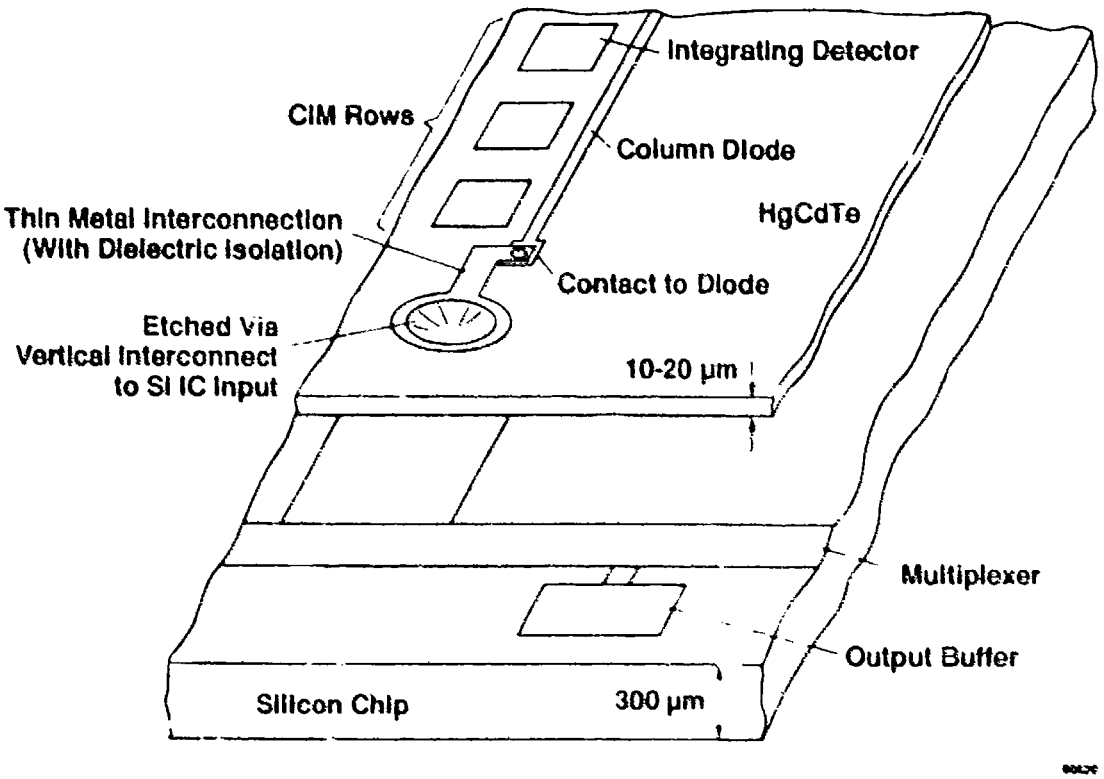


Figure 1-4. Schematic detail of vertically integrated CIM array.

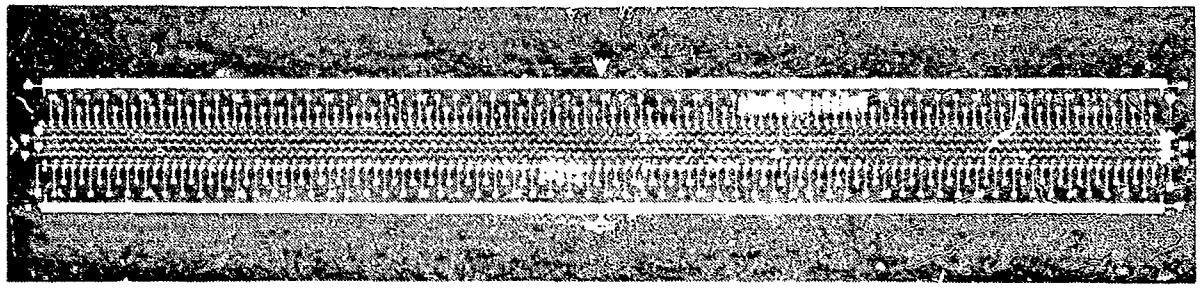


Figure 1-5. Redundant linear version of IRST charge imaging matrix, comprising two independent 480 × 1 arrays.

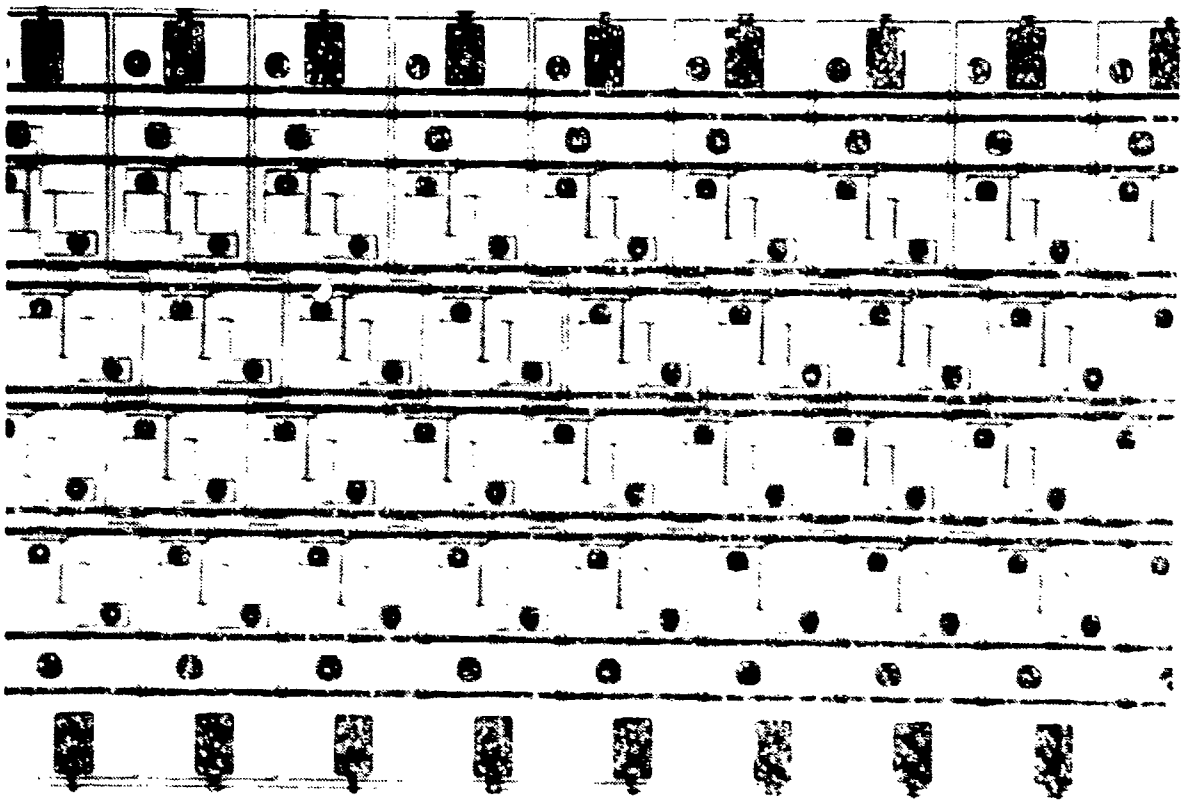


Figure 1-6. Detail of active area of 480 × 1 linear CIM array.

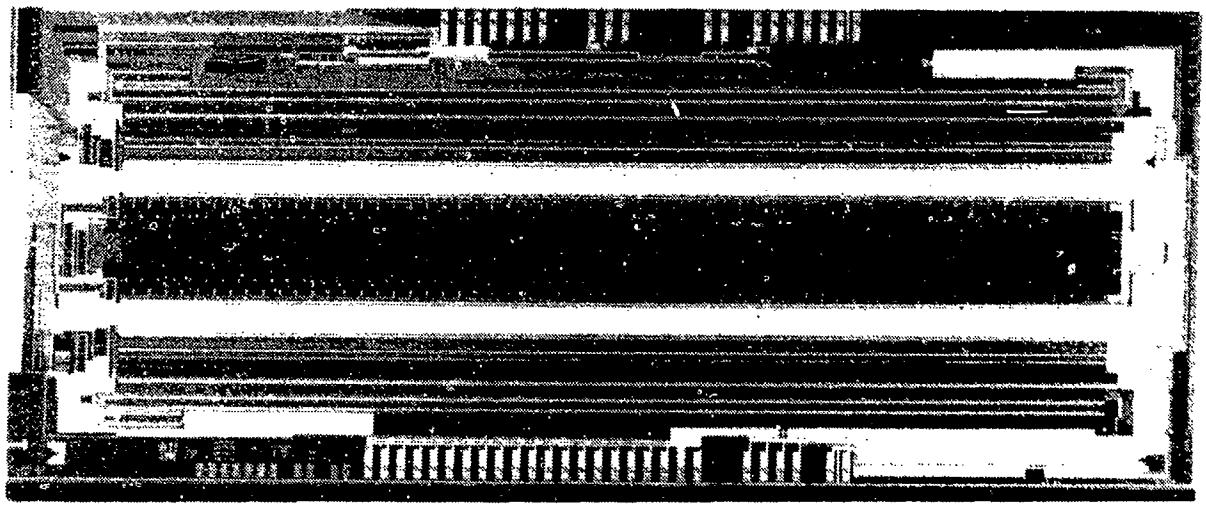


Figure 1-7. Custom-designed silicon IC processor for 480 × 1 linear version of IRST CIM array.

The array-development phase of the program consisted of several major tasks:

1. Design of the 480 × 4 and 480 × 1 IRST CIM detector arrays
2. Implementation of advanced CIM process technologies for enhanced array yields and producibiiity. Process development, including extension of the CIM fabrication technology to vertically integrated architectures, was outside the program scope and was conducted on internal funding.
3. Design, fabrication, and characterization of two custom Si IC processors
4. Design and fabrication of custom focal-plane ceramic chip carriers and interconnects
5. Design and assembly of a scanning CIM test station, including Dewar module, focal-plane electronics and optics, external driver and processing circuitry, and system control software
6. Array demonstration.

The technology-study phase of the program consisted of:

1. Fabrication and screening of CIM test-structure lots, using the CIMTEK test-bar design developed on the previous program
2. Single-pixel CIM detector noise analysis
3. Diode leakage and noise-reduction studies, including an investigation of diode 1/f noise
4. Investigation of the MIS properties of thinned p-type HgCdTe substrates for vertically integrated CIM fabrication.

Elements of the IRST array design are described in Section II. The CIM technology study is discussed in Section III, and the remaining aspects of the IRST array development are presented in Sections IV through VII. Section VIII provides summary and conclusions.

SECTION II
IRST ARRAY DESIGN

A. CIM ARRAY CONCEPT

A charge imaging matrix (CIM) pixel consists of four elements, as shown in Figure 2-1. The central element is a metal-insulator-semiconductor (MIS) detector (photocapacitor) with a semitransparent gate electrode for collecting photon-generated charge during a fixed integration period τ_i. The gate electrode may be all semitransparent, as in the figure, or may include an opaque segment for enhanced MIS storage capacity. A narrow diode channel adjacent to the detector serves as an output node for charge sensing, multiplexing, and extraction from the focal plane. An opaque MIS transfer gate isolates the active region from the sense diode and controls charge transfer between the two. The MIS field plate controls the surface potential and electric fields at the edges of the MIS detectors and diode channels to optimize their electrical characteristics.

In CIM operation, the transfer gate is dc-biased into slight depletion to provide a channel for transferring charge from the detector region to the sense diode. To detect IR photons, the MIS region is biased into deep depletion, forming a potential well under the detector gate, as shown in Figure 2-2. This bias condition is maintained for an integration period τ_i, during which photons absorbed in and near the well generate excess minority carriers that collect in the well. Just before the end of

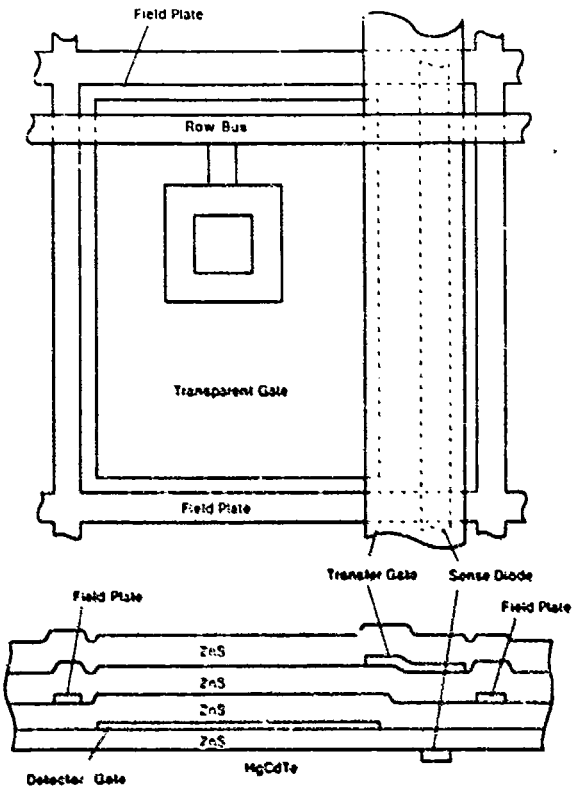


Figure 2-1. Typical CIM pixel architecture.

integration, the sense diode is reset and allowed to float. The detector gate is then momentarily pulsed into accumulation, collapsing the potential well and causing the stored charge to transfer to the diode, abruptly changing its potential. This sequence is illustrated in Figure 2-2. The change in diode potential is proportional to the incident IR flux and is the signal of interest. It is sensed and amplified with an on-focal-plane signal-processor IC.

After the signal is acquired by the amplifier circuit, the sense diode is reset to a fixed reference potential to remove the photogenerated charge from the focal plane. This diode reverse bias is maintained during the charge-integration period to serve as an antiblooming drain for any saturated detector elements.

In a focal-plane array, CIM detector gates are connected serially in rows, with sense diodes running between detectors to form columns, as shown schematically in Figure 2-3. All transfer gates are typically connected to a common bus line as shown. In this fashion, m × n CIM arrays with m detector rows and n diode output columns may be configured. Metal pads at the ends of the detector buses, diode columns, and transfer-gate and field-plate buses (the latter not shown in the figure) may be used for vertical interconnection to an underlying silicon processor, or for conventional wire bonding in a side-by-side array/processor configuration.

In focal plane applications,[3,4] the detector rows may be scanned electronically or optically, and the diode columns are multiplexed with off-chip circuitry. For optimum efficiency, the MIS detector rows are allowed to integrate most of the time, but their potentials wells are periodically collapsed, in row sequence, to transfer charge from the pixels in a column to the adjacent sense diode. For staring array applications,[3,5] electronic row scan is most efficient and is accomplished using dedicated Si IC row drivers. For scanning array applications, optical row scan is employed, and the CIM rows are clocked synchronously with the optical scanner (usually a rotating mirror system) to produce a line-scanned image. Since the number of detector rows in a scanning CIM is small, row clocking can be accomplished using circuitry that is easily incorporated on the signal-processing chip, and separate row-driver ICs are not required.

B. SCANNING ARRAY DESIGN

The 10 μm IRST scanning array has several key design features:

(1) Incorporation of both a 480 × 4 TDI array and a fully redundant 480 × 2 linear array (both with oversampling) on the same photomask design, allowing either or both versions to be fabricated in the same process lot

(2) 8-to-1 on-chip output multiplexing for the TDI array and 4-to-1 multiplexing for the linear array

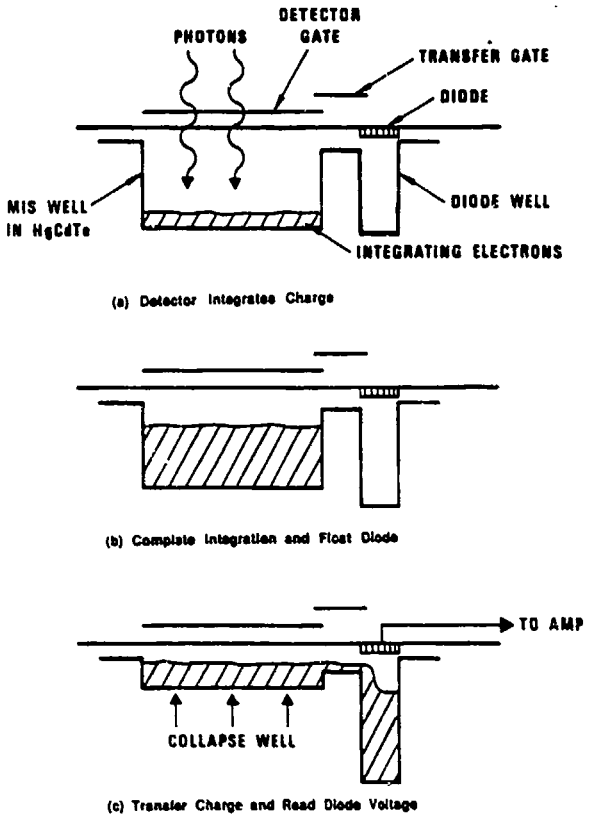


Figure 2-2. CIM operation.

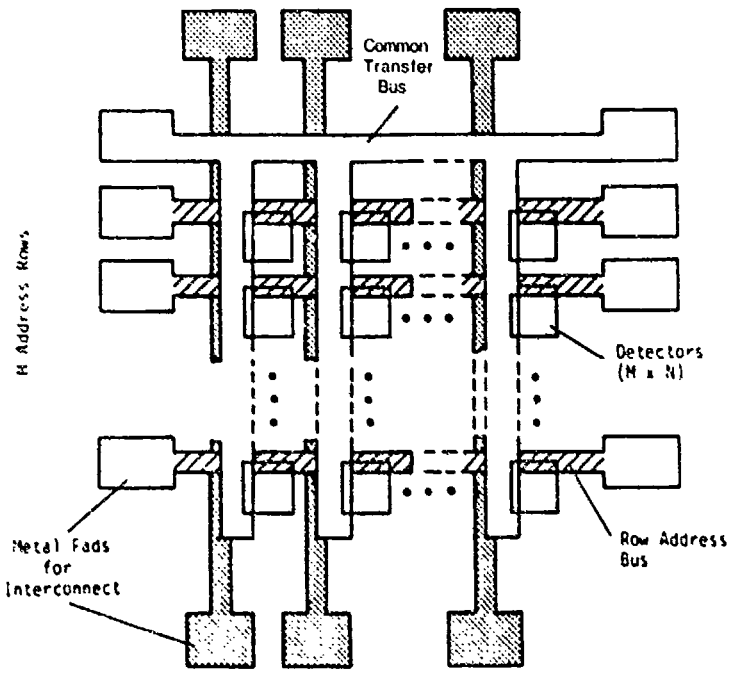


Figure 2-3. Schematic CIM detector array.

(3) Fault-tolerant architecture featuring fusible-link connections to all detector gates for electrical isolation of defective pixels

(4) Segmented field-plate and transfer-gate structures, also with fusible interconnects, for greater fault tolerance of upper-level control gates

(5) Remote vertical interconnections from the CIM diode outputs to the underlying Si processor chip, which provide lower sense-node capacitance and reduced excess noise, as well as eliminate the need for conventional ball bonding to the HgCdTe

(6) Optional bondable version of both arrays, for conventional bonding to existing Si processor chips or for diagnostic testing and evaluation

(7) Optional open-window pixel design for enhanced quantum efficiency and responsivity.

The 480 × 4 TDI array was designed specifically to meet the HARPSS system requirements, and the 480 × 1 (× 2) redundant linear array was designed as a simplified version of the same basic structure.

1. Array Layout

Overall layout of the 480 × 4 TDI CIM is shown in Figures 2-4 and 2-5. The array is configured in eight rows of 240 detectors each, arranged so that each of the top four rows overscans the pixels of the corresponding row in the lower four. Pixel spacing is 3 mils in cross-scan, yielding an active-area length of 720 mils. Overall array length, including row-bus interconnections, is 765 mils; overall array width is 100 mils.

Detector elements are configured so that alternating elements of a given row are coupled to separate row-address bus lines, one above and one below the row, as shown in detail in Figure 2-6; there are 16 bus lines in all. This arrangement allows adjacent pairs of elements to be coupled to the same sense diode, as shown in the figure, and results in a 6-mil spacing between diodes. Each diode column extends half the width of the array, so that a total of eight pixels (in stacked sets of four pairs) are multiplexed onto each diode output. Staggered row-address timing permits each of the eight pixels to be read out in some prescribed sequence, and off-chip signal processing sorts and recombines the multiplexed outputs into a 480 × 1 image line scan.

Coupling to the silicon processor chip is accomplished at remote via sites outside the periphery of the CIM active area, both for the diode column outputs and for the detector row-address inputs. These can be seen in Figure 2-4 and are discussed in detail in a subsequent section.

The 480 × 1 (× 2) linear CIM, shown in detail in Figures 2-7 and 2-8, consists of two fully redundant 480 × 1 arrays. Each array comprises two rows of 240 detector elements, arranged so that one row overscans the other. Pixel pitch and array length are identical to the TDI array, but overall array width (combined) is 90 mils. The alternating row-address scheme is also the same,

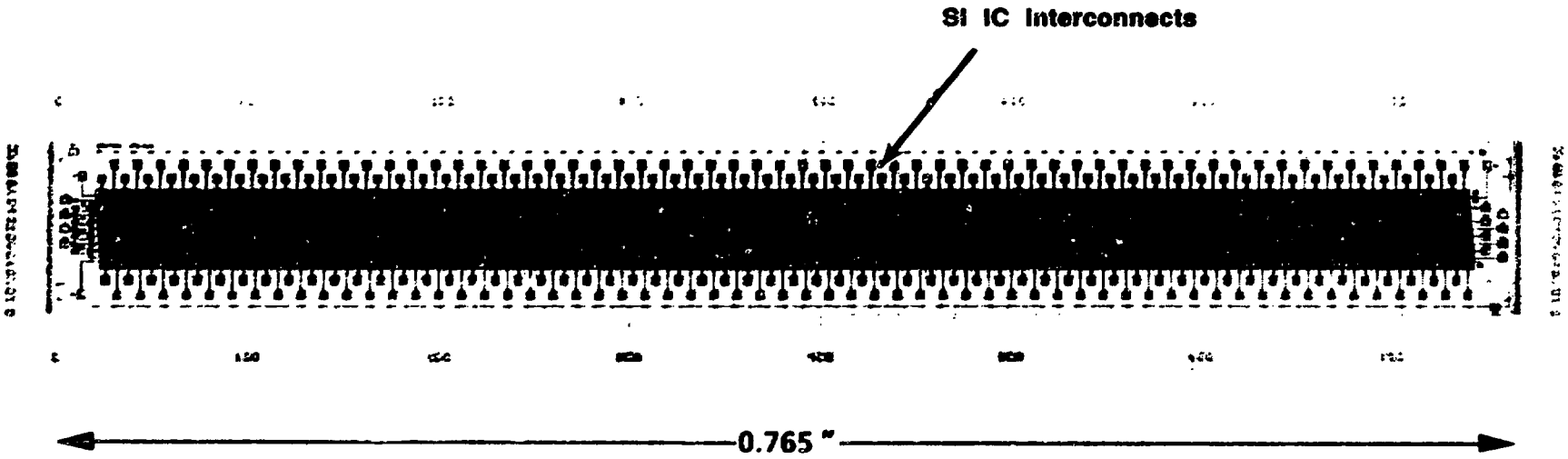


Figure 2-4. 480 × 4 TDI CIM for IRST.

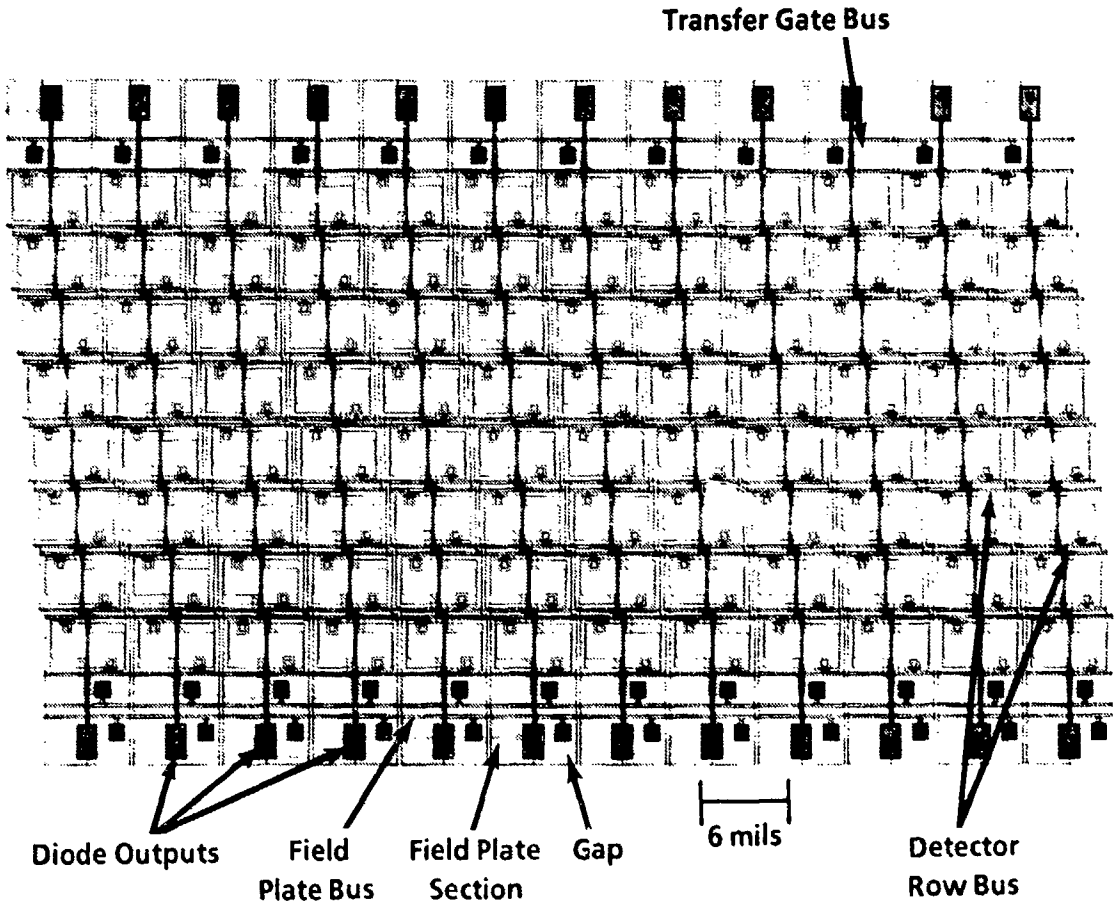


Figure 2-5. Detail of the 480 × 4 IRST CIM design.

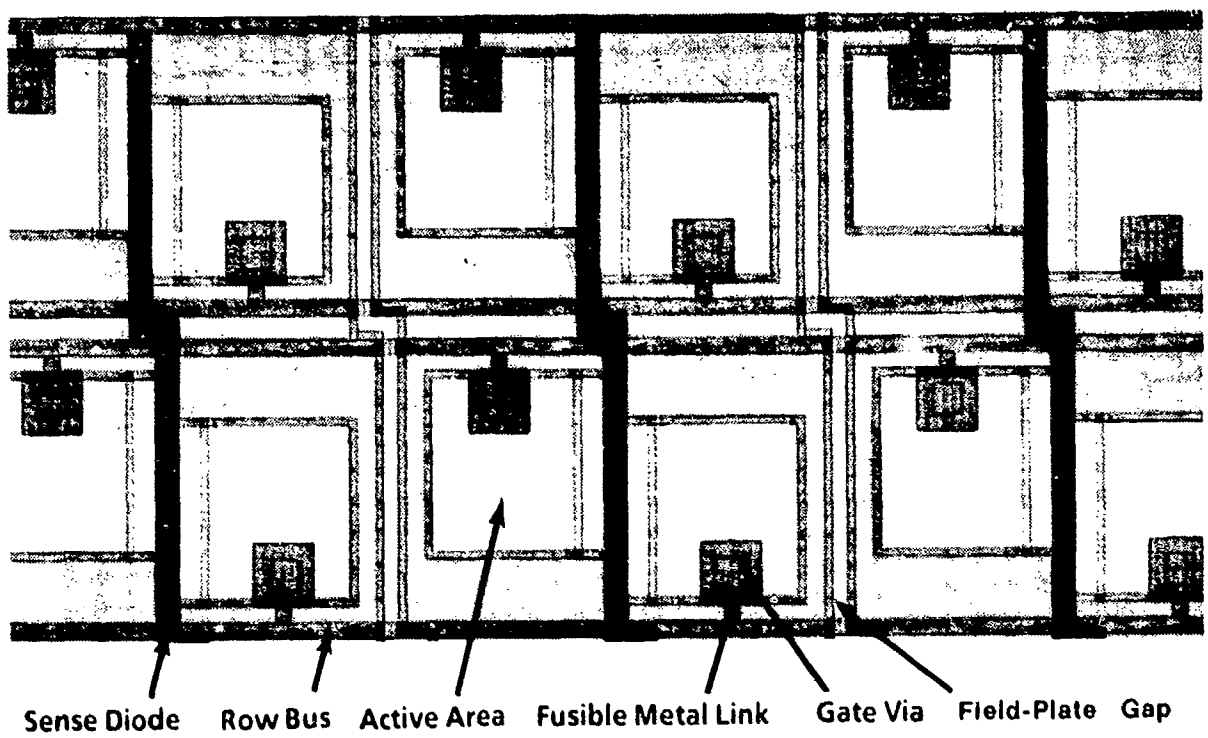


Figure 2-6. Detail of 480 × 4 CIM detector row design.

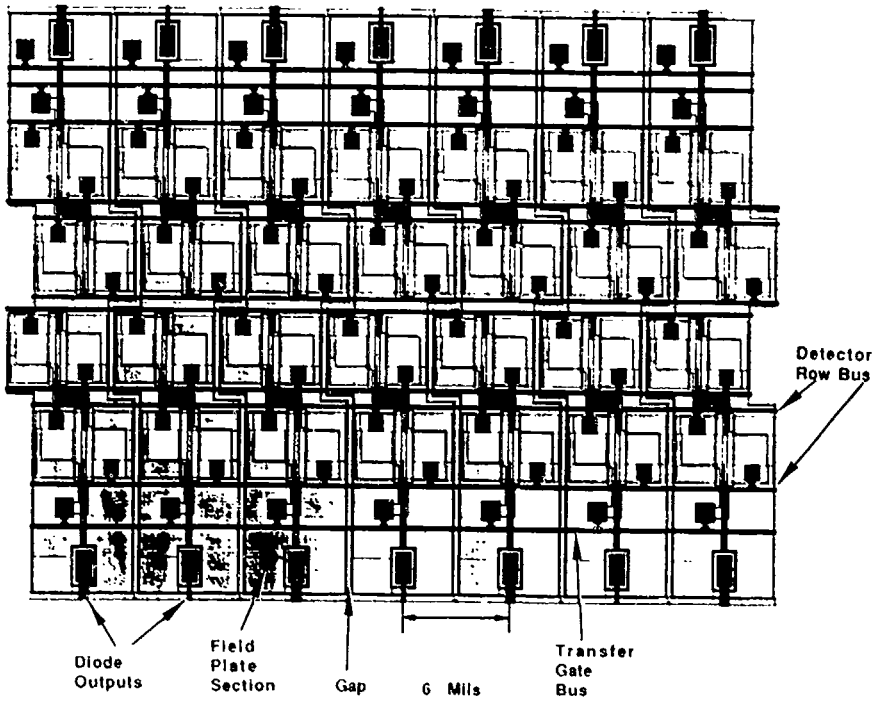


Figure 2-7. Detail of the 480 × 1 (× 2) linear CIM design.

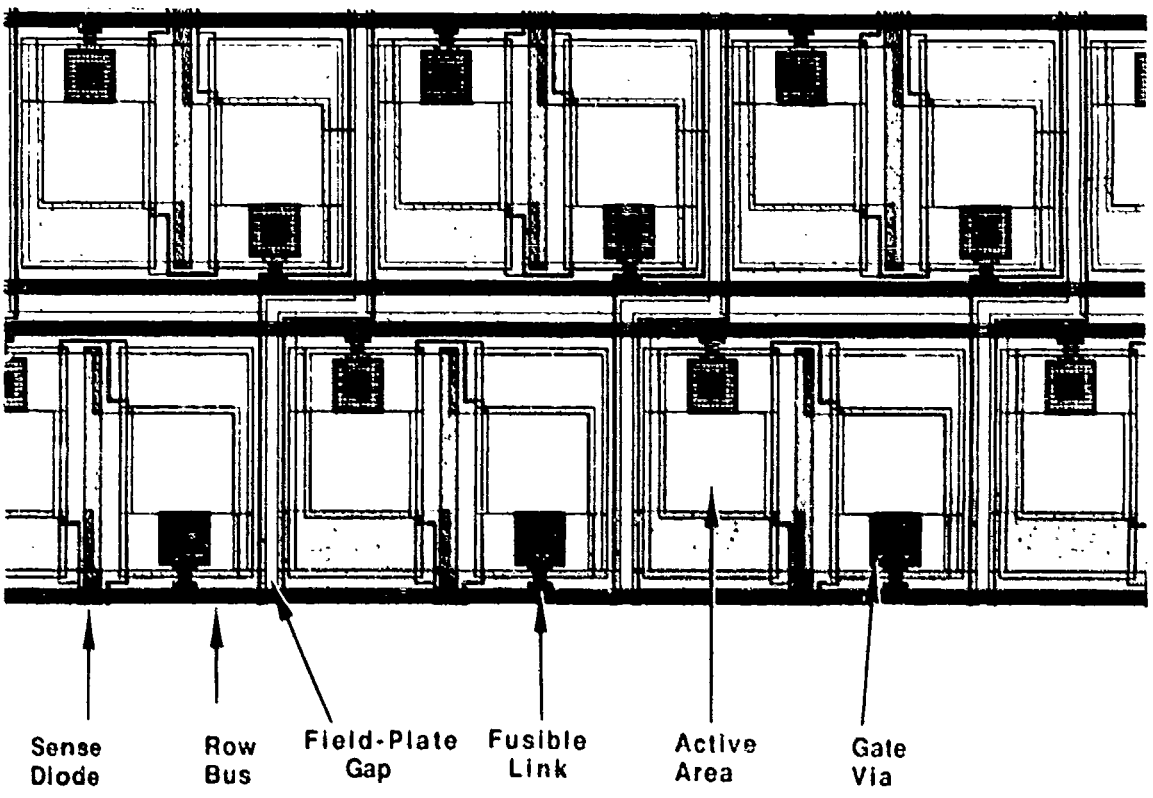


Figure 2-8. Detail of the 480 × 1 CIM detector row design.

except that the linear array requires only eight row buses, and only four pixels are multiplexed on a single diode output, as in Figure 2-9. The two 480 × 1 CIMs are fully independent and may be operated separately or in parallel with suitable off-ship electronics.

The IRST photomask design, shown in composite form in Figure 2-10, consists of one TDI array and one redundant linear array, separated by a strip containing CIM and process-monitor test structures. A typical HgCdTe substrate grown by solid-state recrystallization can readily accommodate one array plus test structures by selection of the appropriate portion of the photomask pattern. Wider HgCdTe samples grown by liquid-phase epitaxy typically can accommodate the entire photomask pattern (and, in some cases, multiple copies of the pattern), providing more than one array per sample. If desired, the test-structure portion of the pattern can be masked off and only the array portion fabricated. On the photomask reticles generated for the GCA direct step-on-wafer (DSW) system, the pattern shown was repeated once; i.e., the composite photomask contained two TDI and two linear arrays, plus two sets of test structures.

2. Pixel Cell Architecture

The TDI CIM pixel is shown in detail in Figure 2-11. The MIS gate measures 2.1 × 2.4 mils and consists of an optically active area 1.6 × 1.7 mils, plus an opaque region with a total area

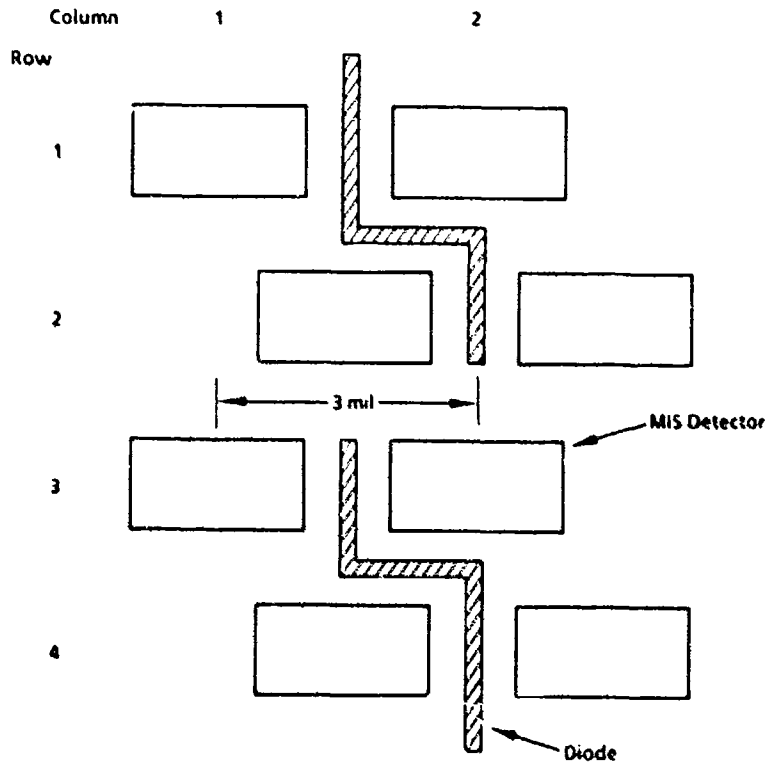


Figure 2-9. Diode multiplex scheme for the 480 × 1 CIM. Four pixels from two columns transfer charge onto each diode.

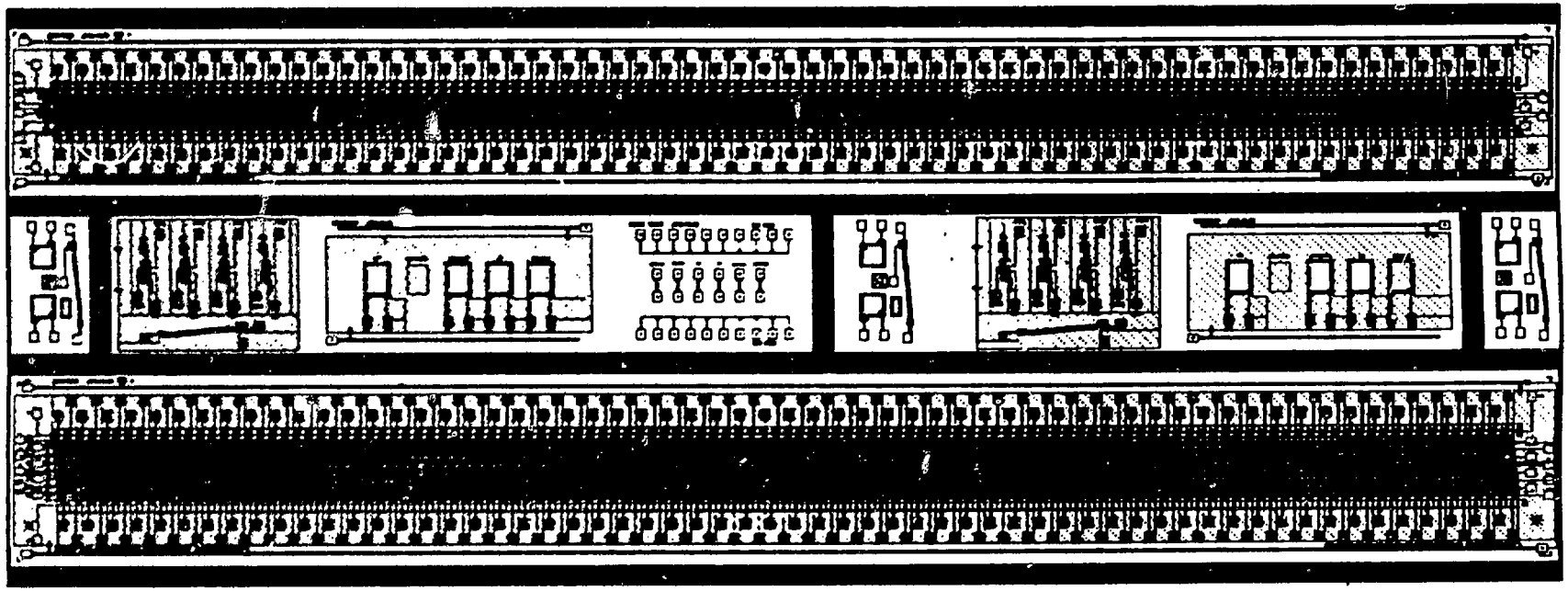


Figure 2-10. Composite plot of IRST photomask design. Redundant linear array is at the top and TDI array at the bottom.

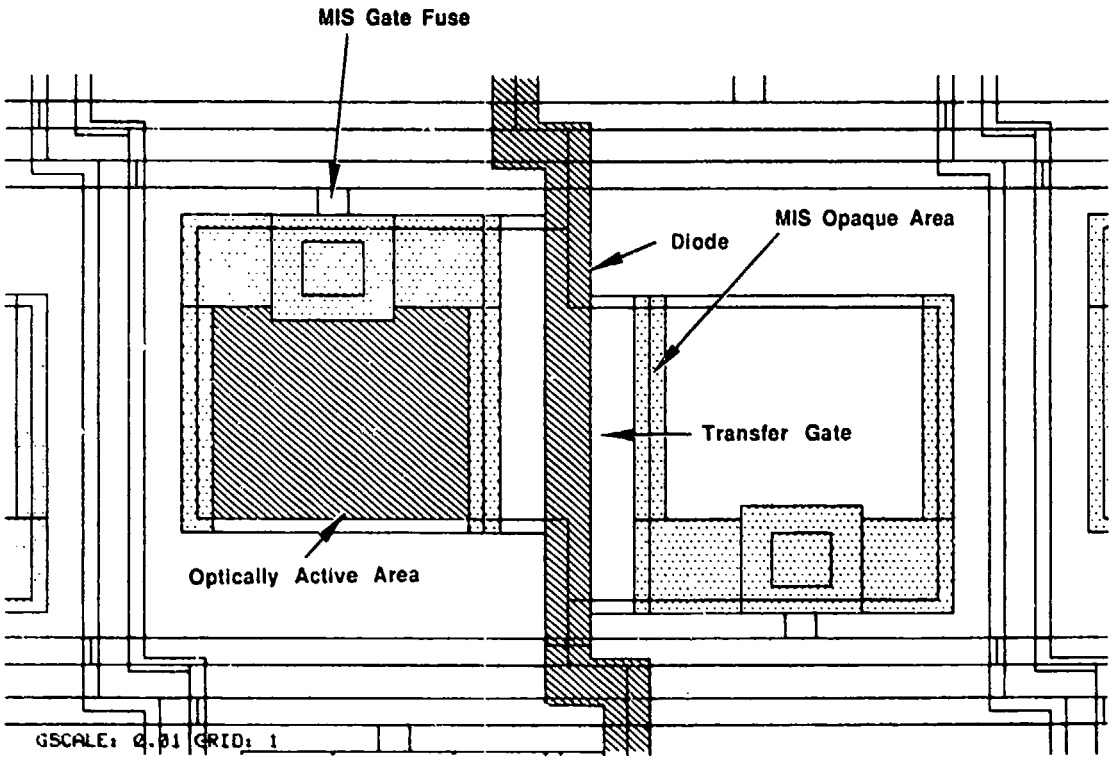


Figure 2-11. Pixel cell design for 480 × 4 TDI CIM array.

of 2.32 mil^2. The latter region provides additional MIS storage capacity as well as a positive stop for the detector gate via. The ratio of storage to optically active area is chosen to optimize detector performance under specified system operating conditions, as described in Subsection II.D, and for the TDI pixel is approximately 1.9. Optical fill fraction in cross-scan is 57%.

The field-plate and transfer-gate boundaries overlap the detector gate by 0.1 mil on all sides to eliminate edge-field effects. The sense diode is 0.3 mil wide and is separated from the adjacent MIS regions by 0.3 mil. The diode is covered by transfer-gate metal in the region between pixels and by field-plate metal elsewhere. Bordering the pixel opposite the diode column is a 0.2-mil gap between field-plate segments, covered by 0.4-mil width of transfer-gate metal to serve as an optical shade.

Each MIS gate is connected to its corresponding row-address bus by a thin fusible link, indicated in the figure. The fusible links are designed to permit isolation of shorted elements from the row bus (by selective application of external bias) so that individual defective pixels do not render an entire detector row inoperative. Fusible gate links were first used on the 128 × 128 large-area CIM and were shown to produce significant enhancement of functional array yields.

The linear CIM pixel (Figure 2-12) is similar to the TDI pixel except that optimization of performance parameters for the non-TDI case results in somewhat different sizing. With active

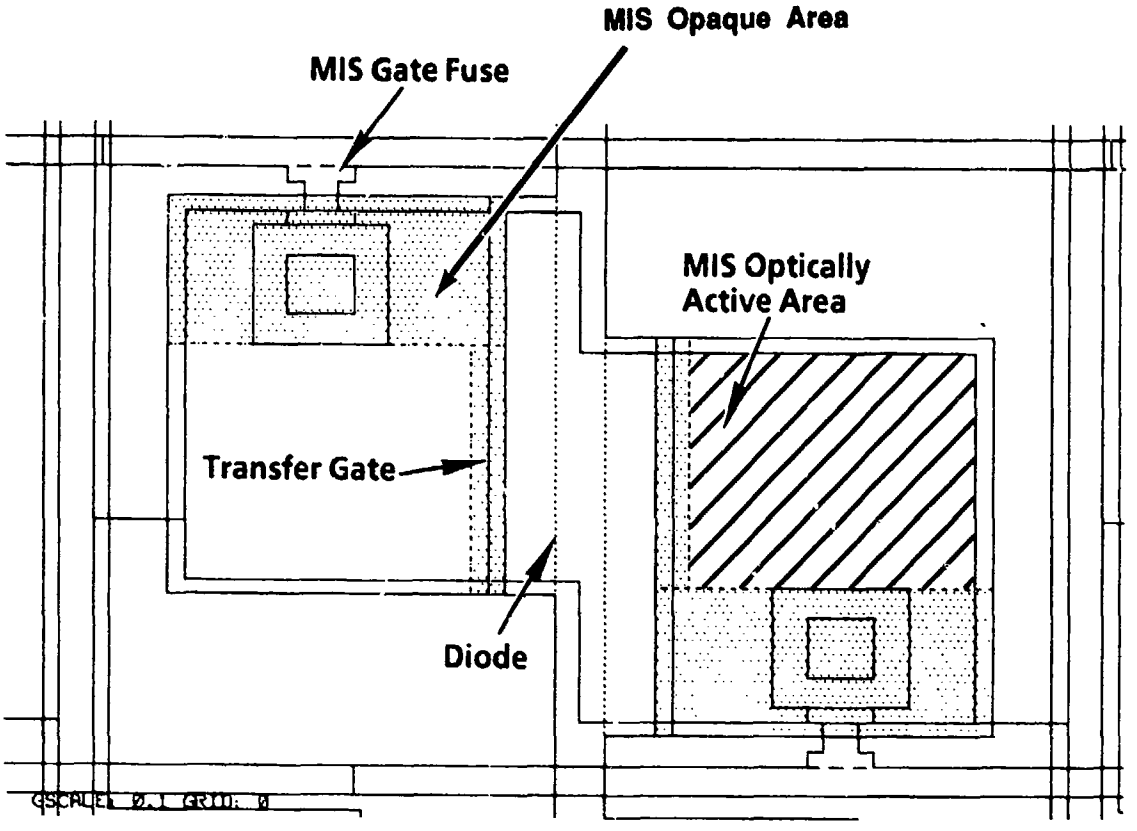


Figure 2-12. Pixel cell design for 480 × 1 linear CIM array.

area chosen to be the same 1.6 × 1.7 mils, total pixel size is 2.0 × 2.7 mils, and the ratio of storage to active area is approximately 2.0. Gate overlaps and other design rules are identical to the TDI case.

3. Segmented Field Plate and Transfer Gate

To enhance CIM yields, the field-plate and transfer-gate structures on both array designs are divided into segments, as indicated in Figures 2-5 and 2-7. The field plate consists of 120 segments 5.8 mils wide and separated by 0.2 mil. Each segment covers a pair of detector columns (16 pixels for the TDI array and 8 pixels for the linear array) with the common diode output running down the center. Each segment is connected by a fusible link to a common bus, as shown in Figure 2-13. The fusible links allow a shorted field-plate segment to be isolated from the rest of the structure and thereby render the remainder of the array operational. Without this feature, a shorted field plate would prohibit operation of any portion of the CIM (unless the passivation process normally produced an accumulated surface on a p-type HgCdTe substrate).

The transfer gate is similarly divided into 240 segments, 120 for each side of the array (or for each array, in the case of the redundant linear CIM). Each segment covers one output diode and is coupled by a fusible link to a common bus, also shown in Figure 2-13. Two transfer-gate buses

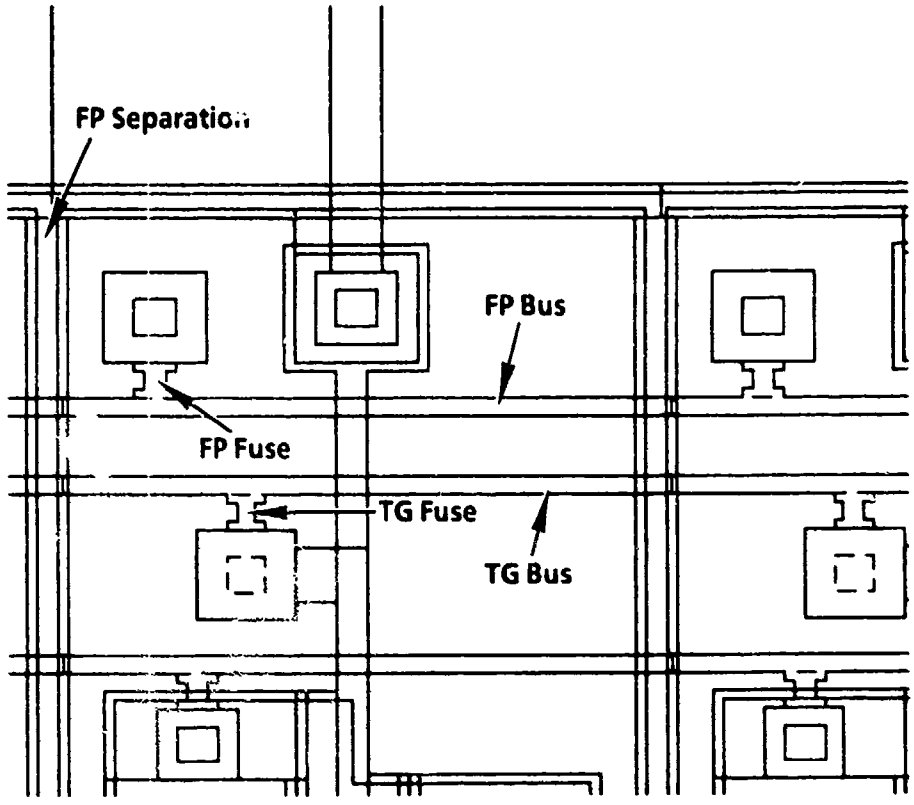


Figure 2-13. Field-plate and transfer-gate bus/fuse detail for 480 × 1 array.

thus are required, one at the top and one at the bottom of the array. Only one field-plate bus is required, and this runs parallel to the transfer-gate bus along one side of the array, as indicated in the figure.

Incorporation of fusible links for all control-gate levels makes the IRST array significantly more fault-tolerant than previous CIM designs. Because of their large gate area, CIM field plates and transfer gates were particularly susceptible to electrical defects and were a primary yield-loss mechanism on larger CIM arrays. With the present design, isolation of a defective field-plate or transfer-gate segment leaves two detector columns nonfunctional and enables operation of the remainder of the CIM array.

4. Interconnections

On both array designs, diode read lines terminate along the top and bottom edges of the array and row, field-plate and transfer-gate buses terminate at the ends of the array, as shown for the TDI case in Figure 2-14. All bus and diode lines are terminated with HgCdTe vias covered by full-size (4 × 5 mils) indium bond pads, shown in detail in Figure 2-15. This arrangement allows fabrication of IRST arrays either with vertically integrated connections (to an underlying Si processor chip) or in conventional monolithic fashion (with indium ball bonding to outboard processor circuitry). The vertically integrated CIM (VICIM) option requires the addition of three photomask levels to form the vias at each of the interconnection sites.

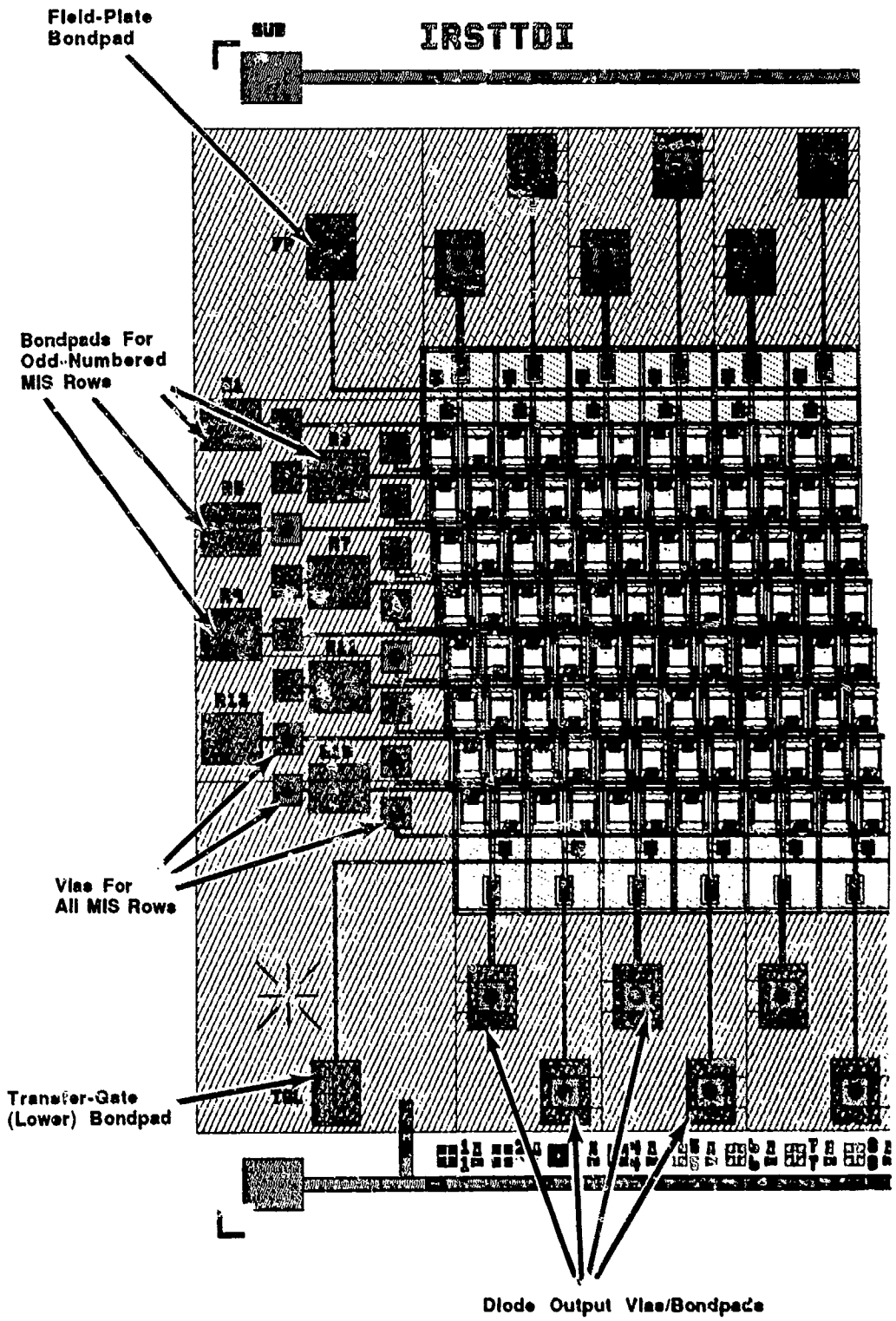


Figure 2-14. One end of 480 × 4 TDI array showing combined via/bondpad scheme for diode outputs and MIS control gates. Field-plate and transfer-gate vias are at the opposite end of the array.

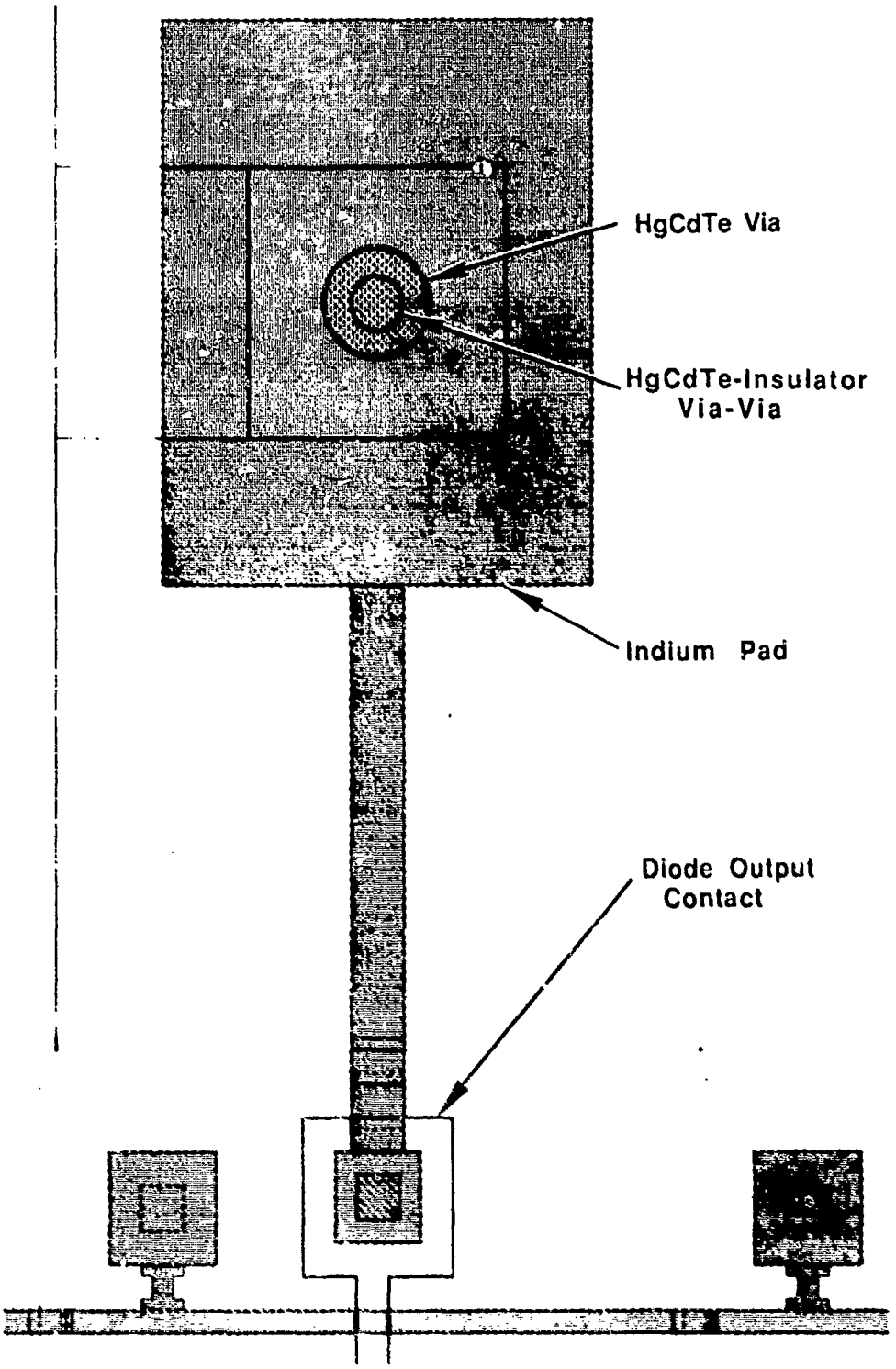


Figure 2-15. Via/bondpad interconnect for CIM IRST arrays. Indium interconnect is large enough to serve as bond pad for gold wire bonding. HgCdTe via and via-via (for first insulator) are at center of interconnect.

To provide sufficient spacing for gold-wire bonding, the bond-pad arrangement is staggered (Figure 2-16). Neighboring diode-output pads are staggered by 7.5 mils in the scan direction, and the width of the bond-pad bus is adjusted to give the same parasitic capacitance for both, as shown in the figure. For the MIS rows, the bond-pads and via sites are separated (as in Figure 2-14); all vias are clustered at one end of the array (matching the Si processor design), while the bond pads are divided, with half at each end of the array, for ease of bonding. This scheme produces a higher parasitic capacitance that is negligible compared with the detector row capacitance (typically >100 pF). The same scheme applied to the diode outputs, however, would produce a significant increase in output node capacitance (typically 3 to 5 pF for the vertically integrated case).

Bond pads for field plate and transfer gate are located at the corners of the array (Figure 2-14), with the corresponding vias at the opposite corners (not shown in the figure). Substrate-contact vias are similarly configured.

5. Test Structures

Test-structure layout for the IRST CIM is shown in Figure 2-17 and includes the following:

(1) Two sets of large-area MIS test capacitors with guard rings, one each for detector-gate (transparent), detector-gate (opaque), field-plate, transfer-gate, and bus/bond-pad levels.

(2) Two sets of single-bit CIMs. Each set contains four identical single-element CIM detectors (with individual diodes, transfer gates, and field plates) of the same configuration as the 480 × 1 linear CIM pixel, plus one independent test diode.

(3) Three "mini-test" sections, each containing two transparent-gate test capacitors and one test diode.

(4) A set of fusible-link test structures and test resistors, primarily for process monitoring.

The initial photomask design also included a set of HgCdTe via continuity and shorting test structures, but these were incompatible with VICIM processing requirements and were later omitted. In the case of monolithic fabrication, the test structures and either the TDI or linear array can be patterned on a typical HgCdTe substrate. For VICIM fabrication, the substrate must be positioned off-center on the Si processor to accommodate the width of the test-structure region; this asymmetric placement was found to cause processing difficulties (nonuniform via formation) and, as a result, the test structures were omitted on later VICIM development lots.

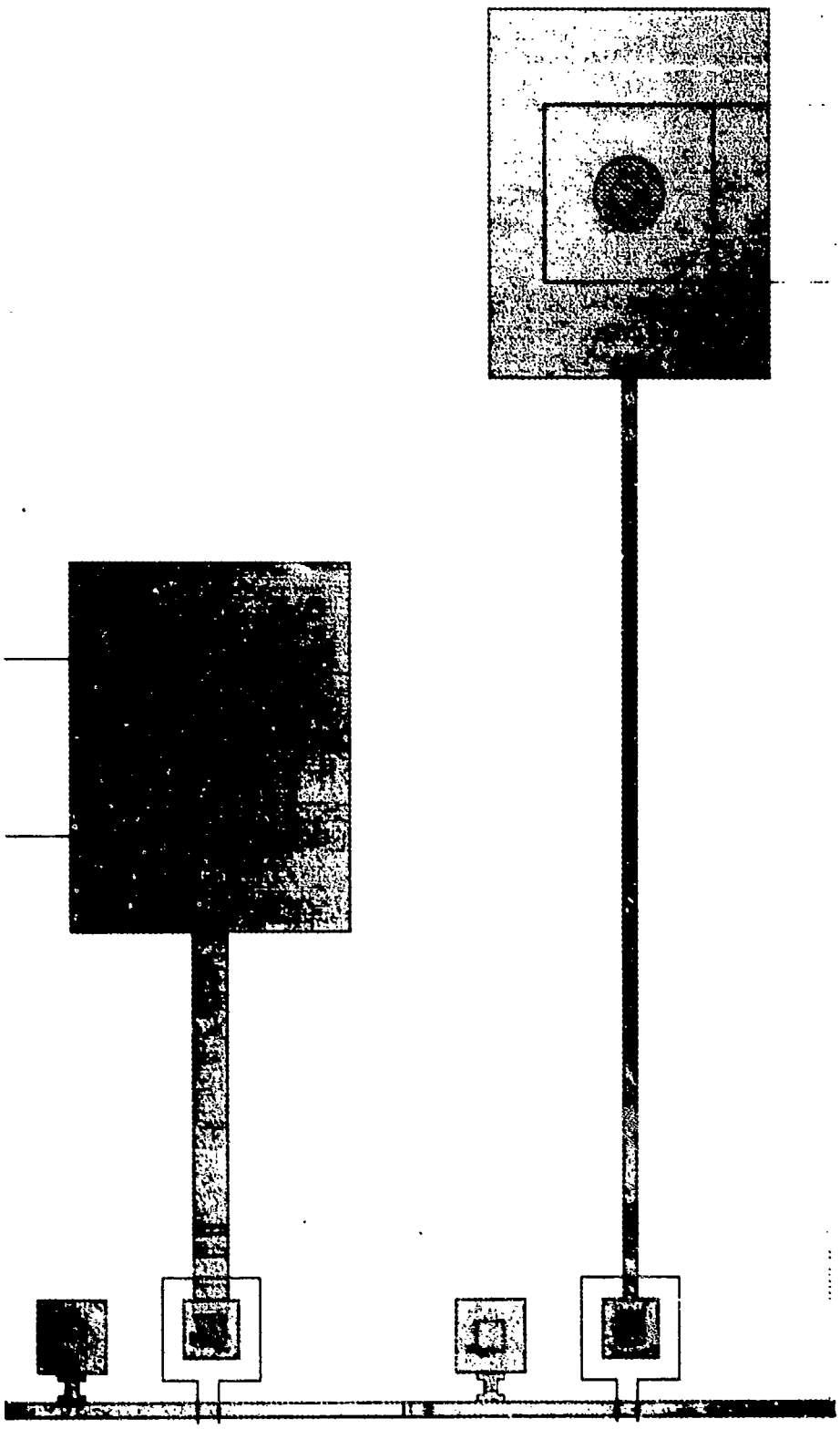


Figure 2-16. Staggered interconnect arrangement for proper pad-to-pad spacing for gold wire bonding.

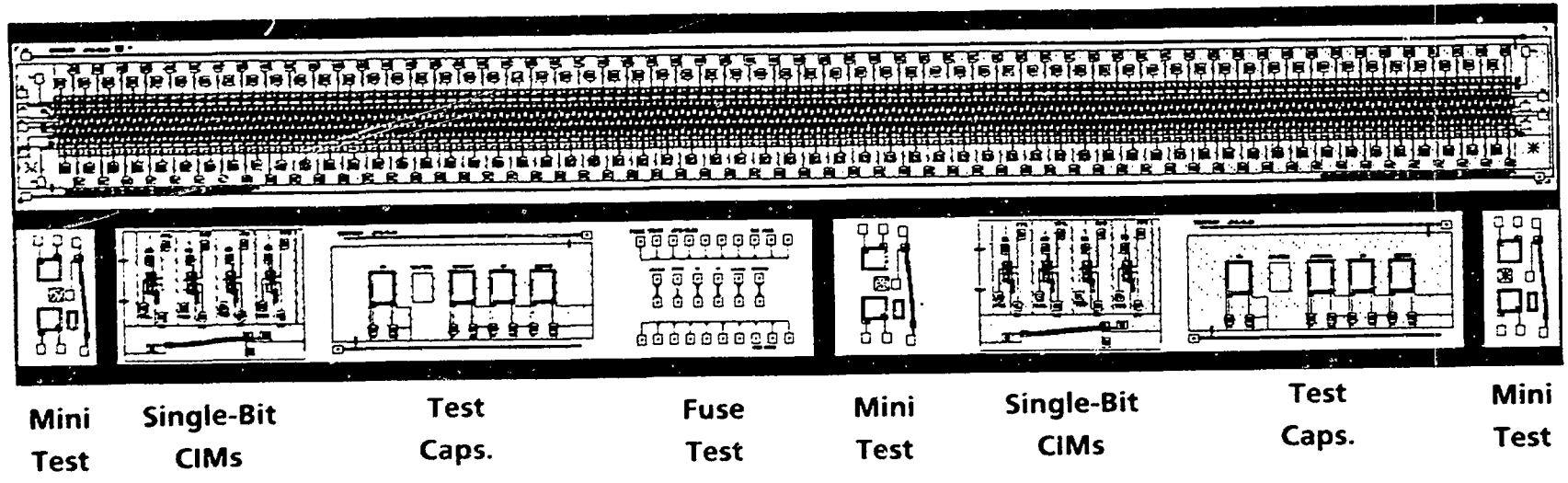


Figure 2-17. Test-structure layout for IRST CIM.

C. DESIGN/FABRICATION OPTIONS

The primary design/fabrication option for the 10-μm IRST array is that of the VICIM versus the monolithic CIM device structure. The former offers clear performance advantages. First, the direct vertical interconnections provide lower sense-node capacitance (by minimizing parasitics) and reduced excess noise, which enhance detector responsivity and sensitivity. Second, by eliminating the need for conventional ball bonding to the HgCdTe, the VICIM focal plane offers greater ease of assembly, lower risk, less heat loading, and enhanced reliability. Also, overall focal-plane size is reduced by elimination of outboard Si processing circuitry and associated interfaces.

The monolithic, bondable version of the array was intended as a development vehicle to demonstrate the feasibility of the 10-μm CIM array concept. It also permitted three program efforts to be conducted in parallel: design and fabrication of the Si processor ICs; development of the vertically integrated fabrication process, including procedures for thinning and backside-passivating p-type HgCdTe substrates; and refinement of the standard (monolithic) portion of the CIM process for array yield enhancement. Bondable arrays were fabricated on unthinned (typically 10 to 20 mils thick) HgCdTe and coupled outboard to existing Si processors using custom-designed ceramic chip carriers. Completed arrays could also be assembled in test packages without processor chips and operated using external circuitry for individual row and column performance analysis and diagnostics.

The 480 × 1 linear CIM also was intended as an intermediate vehicle for array demonstration and analysis. Existing 120-channel Si IC processors were not TDI compatible, and when coupled to the bondable 480 × 4 TDI CIM could be used only for row-by-row detector operation. The same ICs were functionally compatible with the 480 × 1 design, however, and could be used to operate the bondable linear array in a full imaging mode. The linear CIM design would also prove useful for the first VICIM FPA demonstration and would provide a more direct performance comparison with competing (non-TDI) scanning FPA technologies.

Another IRST design option was for open-window MIS gates, in which the semitransparent gate metal is omitted and photogenerated carriers must diffuse to the outer (opaque-gate) storage region to be collected in the MIS well. This configuration, illustrated in Figure 2-18, has the potential for enhanced detector quantum efficiency[6,7] (70 to 80% compared with 40 to 50% for thin-Ni gates), and requires a simple redesign of the CIM pixel involving only three photomask changes. (Since the storage area of the open-window pixel is just the opaque-gate area, the pixel geometry must be altered to give the same storage-to-active-area ratio; this requires minor modification of opaque-gate, field-plate, and transfer-gate geometries). Although these photomask changes were implemented as a fabrication option, the subsequent development of alternative, high-efficiency (75 to 80%) transparent-gate metallizations eliminated the need for an open-window CIM design.

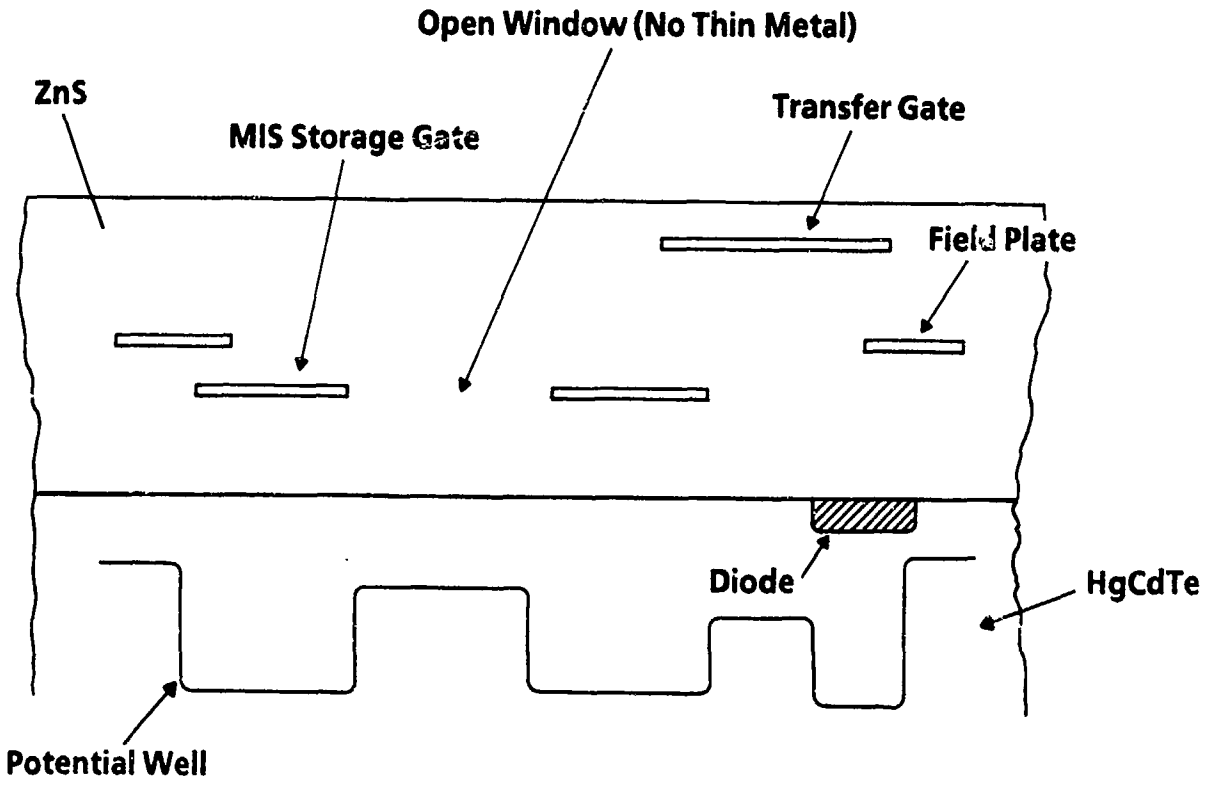


Figure 2-18. Open-window CIM detector.

D. PERFORMANCE PREDICTION

Although it was not a goal of the development contract to meet the FPA requirements for a specific IRST application, the 480 × 4 CIM design was tailored to address the performance requirements of the Navy's HARPSS program. The essential FPA operating constraints were expressed in terms of the system optics and minimum and maximum IR flux levels (for specifieddetector cutoffs) as determined by mission requirements. The 480 × 4 CIM design parameters were then optimized for maximum detector sensitivity, efficiency, and speed under these sets of conditions.

Details of the IRST performance calculation are presented in the Appendix. The essential results of the analysis are expressed in Figures 2-19 and 2-20. These figures plot the predicted CIM sensitivity D_λ^* as a function of MIS storage-to-active-area ratio for different detector cutoff wavelengths. Figure 2-19 assumes an ideal (i.e., zero-leakage) sense diode, and Figure 2-20 assumes a diode leakage current density of 5 mA/cm^2, a typical value for ion-implanted, postannealed diodes in LWIR p-type HgCdTe at reverse bias levels of –0.5 V. Both calculations assume the use of thinned HgCdTe substrates, which can reduce MIS diffusion dark currents by an order of magnitude, and thin-Ni MIS gates having a quantum efficiency of 0.5 (50%).

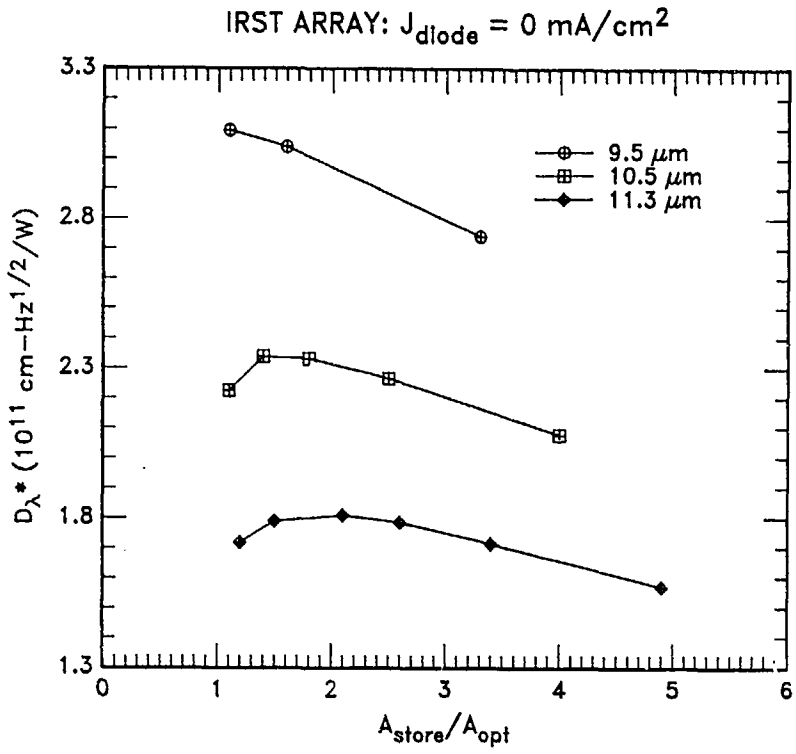


Figure 2-19. **Predicted detectivity versus storage-to-optical area ratio for 9.5-, 10.5-, and 11.3-μm IRST detectors. Diode leakage current was taken to be zero and quantum efficiency to be 0.5 (50%).**

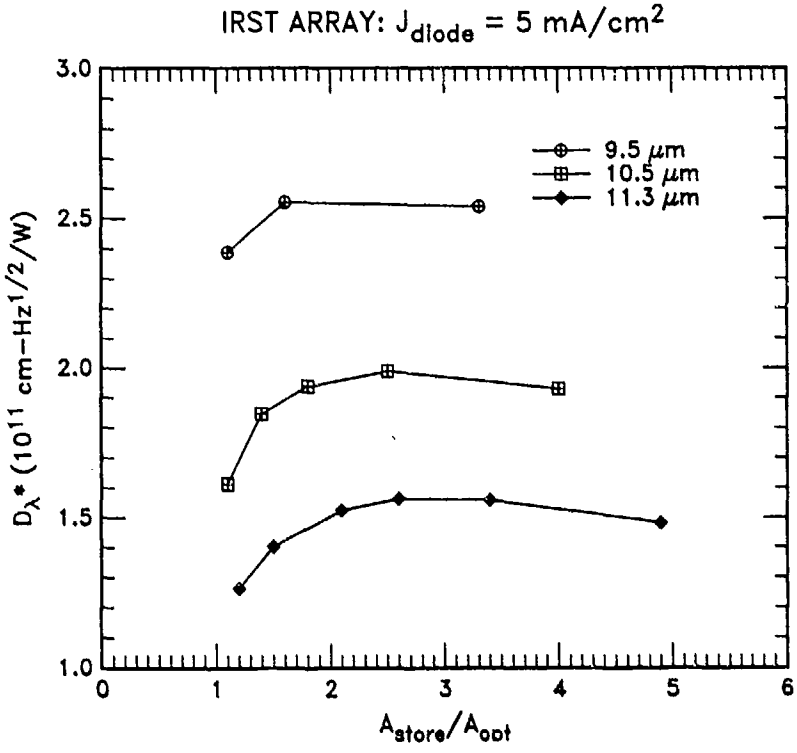


Figure 2-20. **Predicted detectivity versus storage-to-optical-area ratio for 9.5-, 10.5-, and 11.3-μm IRST detectors, for diode leakage current density of 5 mA/cm^2. Quantum efficiency was taken to be 0.5 (50%).**

For the range of cutoff wavelengths shown (9.5 to 11.3 μm), and for diode leakage levels between the extremes considered, maximum predicted detectivity occurs for a storage-to-active-area ratio between about 1.5 and 2.5; the value 2.0 was chosen for the 480 × 4 TDI pixel design. Corresponding D_λ^* for finite leakage current varies from 1.4 to 2.5×10^{11} cm $Hz^{1/2}/W$ depending on detector cutoff, and from 1.8 to 3.1×10^{11} cm$Hz^{1/2}$ for the zero-leakage case. In both cases, shorter cutoff wavelength provides lower MIS dark currents, lower diode leakage, and greater MIS well capacity, and, therefore, results in higher D_λ^*. Corresponding values of noise-equivalent temperature difference (NEΔT), shown in Table 4 of the Appendix, range from 0.014 to 0.021 K.

Performance calculations were also made for optimizatin of the open-window CIM design, assuming a quantum efficiency of 80%. Results for zero diode leakage are shown in Figure 2-21. Comparison with Figure 2-19 shows an overall enhancement in optimum sensitivity of about 25%, or approximately the square root of the ratio of the assumed open-window and thin-Ni quantum efficiencies (0.8 versus. 0.5), as expected. (D_λ^* is a measure of the signal-to-noise ratio and, therefore, varies approximately as the square root of the detector response, itself proportional to the quantum efficiency.) Corresponding NEΔTs for the open-window CIM are as low as 0.012 K for best case (9.5 μm, zero diode leakage).

As explained in the previous subsection, the need for a separate open-window CIM design ultimately was eliminated with the advent of improved detector gate metallizations that offer enhanced quantum efficiency (75 to 80%) without sacrificing MIS storage area or surface-potential control of the optically active region. The new metallization, therefore, provides a direct performance enhancement with the existing thin-gate design (comparable to or exceeding that of the open-window structure), without need for separate design optimization and photomask modifications.

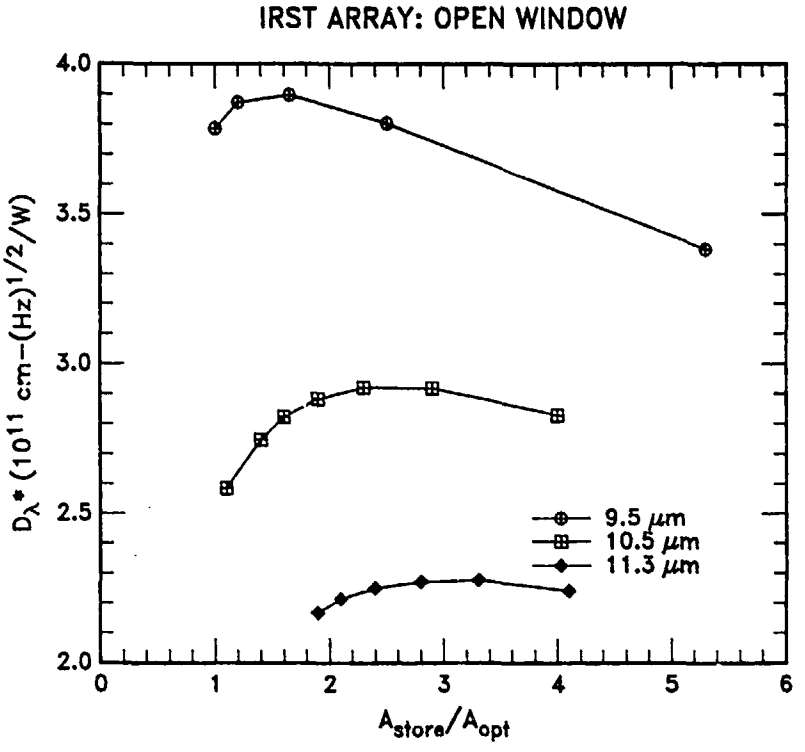


Figure 2-21. **Predicted detectivity versus storage-to-optical area ratio for 9.5-, 10.5-, and 11.3-μm open-window IRST detectors. Diode leakage current was taken to be zero, and quantum efficiency to be 0.8 (80%).**

SECTION III
CIM TECHNOLOGY STUDY

A. INTRODUCTION

Both the MIS photocapacitor and the diode sense node (diode plus processor circuit) contribute to the total noise voltage in a CIM detector. Studies performed under Contract N00014-84-C-2337[1] revealed several key points: (1) the dominant noise contribution for initial 10-μm CIM detectors arose from 1/f and shot noise originating in the ion-implanted HgCdTe diode; (2) the magnitude of this noise rises and falls with diode leakage-current levels; (3) the reduction in 1/f and shot noise achieved using correlated double sampling (CDS), although significant, is limited by the need for adequate processor response time (which sets a lower limit on the clamp-to-sample time interval); and (4) the MIS-well noise contribution can be accounted for by a shot-noise model. The experiments for this last point were performed under the present contract and are described in Subsection III.B.

The companion diode development also performed under the previous contract indicated that postannealing of ion-implanted diodes offers promise for reducing the diode noise contribution in CIM detectors. A reduction of greater than 4× in low-frequency noise-voltage density was demonstrated for a diode baked at 100°C for 16 hours. The leakage-current density for the same diode dropped by a factor of between 6 and 10 depending on the junction reverse bias, which would mean a reduction in associated shot noise by a factor of 2.5 to 3. A net reduction in diode rms noise voltage by a factor greater than 2 would result in a detector with noise dominated by the MIS well contribution and permit background-limited performance.

The technology-study portion of the present program was intended primarily to address the issue of diode leakage and noise reduction using the newly developed anodic sulfide passivation (ASP) combined with the CIMTEK photomask design developed under the previous contract and implemented in the present one. This included the investigation of noise mechanisms in ion-implanted diodes, the refinement of diode baking techniques, investigation of diode characteristics at reduced substrate temperatures, and implementation of postannealed, low-noise diodes on CIM detector arrays. A secondary objective was the investigation of diode and detector uniformity over the long array dimensions required for the IRST application.

An equally important technology issue for vertically integrated CIM (VICIM) array development is the ability to thin p-type HgCdTe to substrate thicknesses required for the vertically integrated fabrication process (about 10 to 20 μm) without degradation of MIS properties. This capability was demonstrated using standard MIS test-structure designs commonly employed for materials characterization, along with surplus LWIR p-type HgCdTe otherwise unsuitable for large-array fabrication.

B. CIM DETECTOR NOISE ANALYSIS

Initial detector noise measurements were performed under the present contract using small (9 × 8) CIM test arrays fabricated and screened under the previous CIM contract. From these measurements, it was concluded that (1) additional detector noise at increased flux levels can be accounted for by photon shot noise; (2) noise associated with the CIM transfer channel is not significant; and (3) all "excess" detector noise can be accounted for by diode leakage-current shot noise, diode 1/f noise, and MIS dark-current shot noise.

Detailed noise measurements were performed on individual elements of a 9 × 8 array having one output column coupled to a single-channel silicon processor located on the focal plane. The signal of a single pixel could be isolated by transferring charge from the other pixels in the column after the sample pulse of the correlated double sampler. MIS well contributions to CIM detector noise could then be evaluated under conditions of varying integration time and flux level. Although the total MIS well charge is a function of both these parameters, variation of signal flux level is necessary to evaluate the contribution from optically generated carriers.

The gain-normalized noise spectrum at 77 K for one element of a 3-mil-pitch, 9 × 8 array for three flux levels is shown in Figure 3-1. The array was operated in a mode appropriate to a high-data-rate, scanned system with preamplifier bandwidth (–3-dB pt) of 1.5 MHz and a clamp-to-sample (read) time of 600 ns. The diode reset voltage was 1.5 V and the MIS integration time was 6 μs. To permit single-pixel detection, the sampling frequency was set at 89 kHz. The optically active area was 4.56 mil^2 and the diode area was 14.4 mil^2. The detector cutoff wavelength (measured at 77 K) was 9.5 μm.

The array in this case was fabricated with unannealed ion-implanted diodes, and the noise spectrum below 1000 Hz is dominated by 1/f noise. Above 1000 Hz, the effects of signal flux can be discerned, the noise-spectrum knee varying from approximately 1000 to 3000 Hz. The noise floor in this region is approximately 110 $nV/Hz^{0.5}$. The measured 1-Hz intercept for the detector 1/f noise was 5.3 $\mu V/Hz^{0.5}$. The noise spectrum of the processor, operated under identical conditions but disconnected from the CIM diode, is shown in the lower trace, with a knee at about 300 Hz.

A good approximation of the total rms noise voltage is obtained by integrating the square of the noise voltage density from 1 Hz to the sampling frequency. The results, as a function of the upper limit of integration, are shown in Figure 3-2. The lower trace shows the integrated noise for the processor only. The integral gives the variance of the noise voltage, and taking the square root yields the rms noise voltages, as tabulated in Table 3-1.

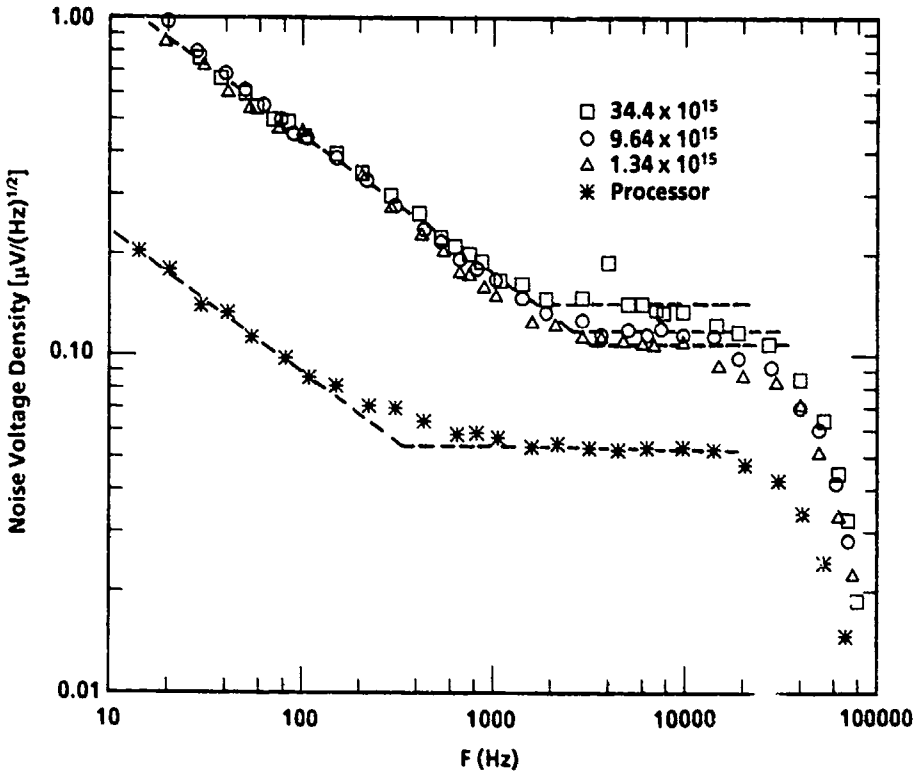


Figure 3-1. Gain-normalized noise voltage spectrum at 77 K for one element of 9 × 8 CIM array (12-3B-1-D). Spectrum measured for three flux levels indicated at sample frequency of 89 kHz. Lower trace is for processor circuit only (disconnected from output diode). Detector cutoff = 9.5 μm.

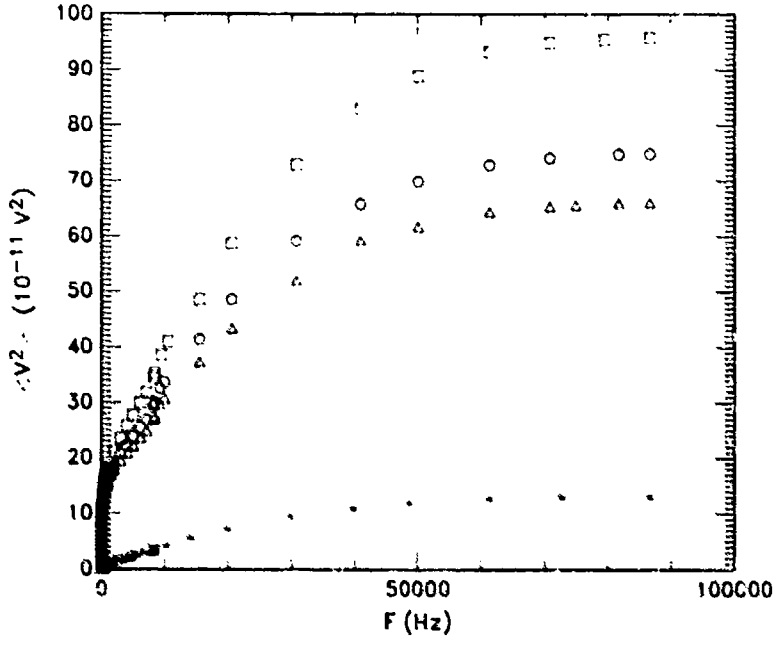


Figure 3-2. Integral of the square of the gain-normalized noise voltage density (from Figure 3-1) as a function of the upper frequency limit for the same three incident flux levels. The lower limit was 1 Hz. The bottom trace is for the processor circuit only (disconnected from the output diode).

Table 3-1. Gain Normalized Total Noise and Photon Noise for Row 1, Diode 8 of CIM 12-3B-1-D

Flux (10^{15} ph/s-cm^2)	Total Noise (μV)	Measured Photon Noise (μV)	Calculated Photon Noise (μV)
1.4	25.7	—	—
9.6	27.35	9.5	8.85
34.4	30.95	17.3	16.7

Because of the very low flux level, the first measurement (25.7 μV) is a good approximation of the "excess" detector noise. This incorporates all contributions other than photon shot noise, including the diode, processor, and MIS-well dark current. The expected photon noise contribution at this flux level is 3 μV, or about 1.5% of the total measured variance or noise power (independent noise components add in quadrature), making this a very good approximation. At the higher flux levels, the measured photon noise is then determined by subtracting (in quadrature) the excess noise from the total detector noise. The theoretical photon noise, shown in the last column of the table, is given by:

$$V_{photon} = \frac{q}{C_N}\left(\Phi\ \eta\ \tau\ A_{opt}\right)^{1/2} \qquad (3-1)$$

where A_{opt} is the optically active area, Φ the incident flux level, η the measured quantum efficiency (18% for this detector), C_N the sense-node capacitance (10 pF), and τ the MIS integration time.

The measured photon noise values are slightly higher than calculated, which may simply indicate that the node capacitance is slightly less than 10 pF. The agreement indicates that the noise contribution from increased signal flux can be accounted for by a shot-noise model, and that additional mechanisms, such as transfer noise caused by charge trapping, are not significant.

The 1/f content of the detector noise can be determined from a plot of integrated noise power density versus frequency,[8] shown in Figure 3-3 (an expansion of the low-frequency region of Figure 3-2). Extrapolation of the linear regions to zero frequency indicates that the 1/f noise voltage is independent of flux level, with an rms value of 13 μV. Earlier work[1] showed that this type of noise originates in the ion-implanted diode. Integration of the processor noise component (from Figure 3-2) yields an rms noise voltage of 11.4 μV. The diode leakage-current and MIS dark-current shot noises were not measured directly but can be calculated from measured dark currents (from storage-time and I-V measurements) to be 15 μV and 11 μV, respectively. (The MIS dark-current density was 380 μA/cm^2, the diode leakage current was 0.24 μA at 0.15 V reverse bias, and the node capacitance was taken as 10 pF). Adding these noise contributions, the expected excess detector noise (Table 3-2) is 25 μV. This is in excellent agreement with the measured value of 25.7 μV (Table 3-1) and indicates that all significant CIM noise sources have been accounted for.

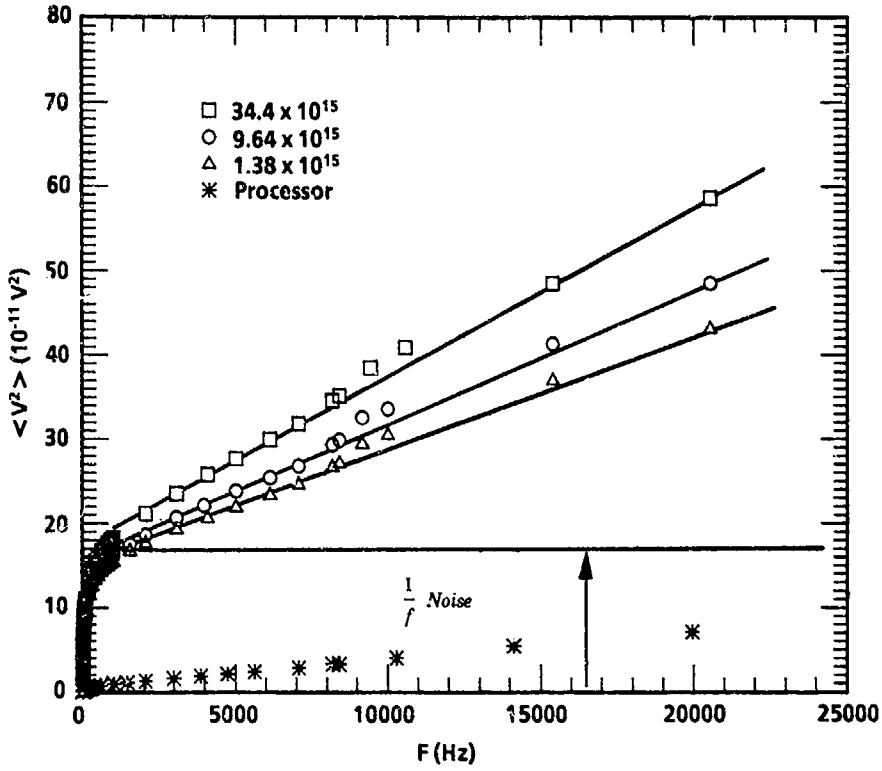


Figure 3-3. **Integral of the noise spectra of Figure 3-1 shown in greater detail. Extrapolation of the linear regions to 0 Hz gives the 1/f component of the total detector noise. The bottom trace again is for the processor only.**

Table 3-2. Excess Detector Noise Contributions for CIM 12-3B-1-D

Source	Contribution (μV)	Comments
1/f	13	Measured
Diode shot	15	Calculated
MIS dark current shot	11	Calculated
Processor	11.4	Measured
Total	25	Calculated

Using these noise data, the detectivity D_λ^*, the commonly used detector figure of merit, may be calculated for the given CIM pixel. The detectivity (at wavelength λ) is defined by:

$$D_\lambda^* \equiv \frac{V_{sig}}{v_{f,s}} \frac{1}{\Phi A_{opt}^{1/2}} \frac{\lambda}{hc} \qquad (3-2)$$

where V_{sig} is the CIM signal voltage (response to a chopped signal flux), $v_{f,s}$ is the sampled noise voltage density (at some frequency f in the flat portion of the noise spectrum), h is Planck's constant, and c is the speed of light. The measured (gain-normalized) signal voltage at a signal flux level of 3.4×10^{16} ph/cm^{2}s was 16.2 mV, which yields a D_λ^* of 3×10^{10} cm-Hz$^{0.5}$/W at 9 μm and 10 kHz.

For a CIM detector, the theoretical detectivity (assuming that photon shot noise is the only noise source) is given by:

$$D_\lambda^*\ (CIM) = \frac{\lambda}{hc} \left(\frac{\eta\ \tau\ f_s}{2\ \Phi_{sig}} \right)^{1/2} \qquad (3-3)$$

where f_s is the sampling frequency. If the optimum quantum efficiency is taken as 0.5, the theoretical D_λ^* is calculated to be 8.9×10^{10} cm-Hz$^{0.5}$/W. The measured CIM pixel, therefore, achieved about 33% of its optimum detector performance.

C. DIODE NOISE REDUCTION

Diode studies performed under the previous CIM development program[1] suggested that postfabrication annealing of ion-implanted diodes could effectively reduce diode leakage and 1/f noise. These studies were extended in greater detail under the present contract using Texas Instruments recently developed anodic-sulfide surface passivation, a proprietary process that produces a thermally stable interface that permits postannealing for many hours at 100°C with little or no degradation in MIS properties.[9] The present study also employed device structures from the CIMTEK photomask design, developed under the previous contract, which incorporates an upper-level field plate for improved device yields and reliability.

Diode characteristics were measured over a range of operating temperatures to identify the various component mechanisms of leakage currents and associated noise. The main conclusions of this study were:

(1) The tunneling component of diode leakage, which dominates for temperatures below about 65 K, is greatly reduced by postannealing at 100°C in nearly all cases.

(2) Diode leakage current is diffusion-limited to below 60 K in many cases following postanneal.

(3) At 77 K, diode leakage at high reverse bias levels (0.8 V) is greatly reduced.

These results have two important implications for 10-μm CIM performance. First, the reduction in leakage currents will mean a corresponding reduction (especially at reduced operating temperatures) in diode shot noise, which contributes significantly to excess detector noise during the time interval from reset to sample. Second, the significant reduction in leakage at high bias levels will allow the use of higher diode reset potentials, which give greater diode charge capacity without the penalty of increased node capacitance.

In addition, the dependence of 1/f noise on diode geometry was investigated to ascertain the probable sources of 1/f noise in ion-implanted diodes. These experiments are described in Subsection III.D.

1. Test Structures

Test structures used for diode annealing studies were contained on the upper one-third of the CIMTEK photomask design (Figure 3-4). The left portion of the pattern contains (among other structures) an 8 × 8 SMALLCIM array and two large-pixel (LP) strings, each string consisting of five equivalent MIS gates coupled (by individual transfer gates) to a common long output diode, and sharing a common field plate. The right portion contains an identical 8 × 8 array and two small-pixel (SP) strings, configured similarly to the LP structures but having smaller geometry. The LP structures have an MIS gate area of 18 mils^2 and the SP structures a gate area of 10 mils^2. Diode area is 56.2 mils^2 for the LP strings and 32.2 mils^2 for the SP. The right portion of the pattern also contains a collection of large-area test diodes of varying perimeter-to-area ratios.

Most of the diode annealing studies were performed using the SP and LP pixel strings. MIS gates could be isolated from the diode channel by appropriate biasing of the transfer gates and the MIS and diode characteristics studied separately; or the strings could be operated as five-element, large-pixel CIM detectors having diode output channels of varying length.

2. Leakage-Current Mechanisms

The three principal mechanisms contributing to for diode leakage current are bulk minority-carrier diffusion, generation-recombination (g-r) current in the diode depletion region, and a thermally assisted tunneling mechanism in the depletion region. The contribution resulting from diffusion of electrons from the p-side of the junction is given by[10]:

$$J_{diff,n} = q\left(\frac{D_n}{\tau_n}\right)^{1/2} \frac{n_i^2}{N_A} \qquad (3-4)$$

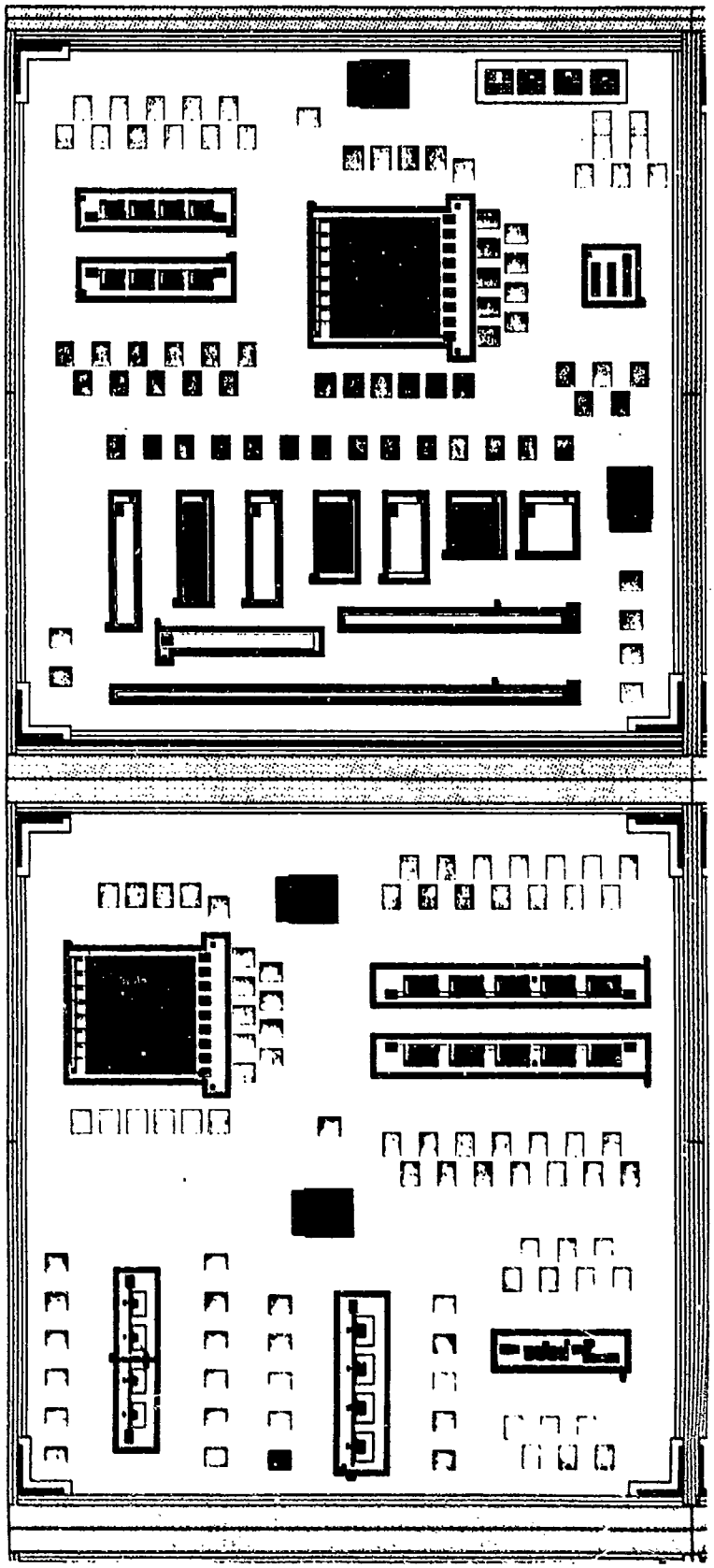


Figure 3-4. Portion of the CIMTEK photomask design containing test structures used in CIM diode studies.

and that resulting from diffusion of holes from the n^+ side is given by:

$$J_{dif,p=} q\left(\frac{D_p}{\tau_p}\right)^{1/2} \frac{n_i^2}{N_d} \qquad (3-5)$$

Here, $J_{dif,n(p)}$ is the electron (hole) diffusion current density, n_i is the intrinsic carrier concentration, N_a is the ionized acceptor density in the p-region, N_d the ionized donor density in the n^+ region, $D_{n(p)}$ is the electron (hole) diffusion constant, $\tau_{n(p)}$ is the electron (hole) bulk minority-carrier lifetime, and q is the electronic charge. The diffusion current is not a function of the junction bias (reverse bias conditions) and, since $N_d >> N_a$, the hole contribution is not significant.

The generation-recombination current density is given by:

$$J_{gr} = \frac{1}{2} q \frac{n_i}{\tau_o} W \qquad (3-6)$$

where W is the junction depletion width and τ_o is the effective depletion-region carrier lifetime. The term J_{gr} depends on junction bias through the dependence on depletion width. If an abrupt junction is assumed, the bias dependence will be given by:

$$J_{gr} = \left(\frac{q\varepsilon}{2N_a}\right)^{1/2} \frac{n_i}{\tau_o}(V + \Phi_{bi})^{1/2} \qquad (3-7)$$

where ε is the semiconductor dielectric constant, V is the applied bias across the junction, and Φ_{bi} is the junction built-in potential.

Finally, the thermally assisted tunneling current mechanism will generally depend on junction bias in an exponential fashion.[11]

For temperatures high enough that carrier freeze-out effects are not important, the diffusion and g-r currents vary with temperature through the intrinsic carrier concentration n_i. Using the nondegenerate band approximation, the corresponding current densities in each case reduce to

$$\ln(J_{dif}) = \ln\left[q\left(\frac{D_n}{\tau_n}\right)^{1/2} \frac{N_c N_v}{N_a}\right] - \frac{E_g}{kT} \qquad (3-8)$$

and

$$\ln(J_{gr}) = \ln\left[\frac{q}{2}\frac{W}{\tau_o}(N_c N_v)^{1/2}\right] - \frac{E_g}{2kT} \qquad (3-9)$$

Here N_c and N_v are the effective densities of states at the conduction and valence band edges, respectively, and E_g is the bandgap energy. Ignoring the slow temperature dependences of $\ln(N_c)$ and $\ln(N_v)$, the temperature dependence of $\ln(J_{dif})$ and $\ln(J_{gr})$ should be linear with slopes of $-E_g/k$ and $-E_g/2k$, respectively. It has been shown experimentally that tunnel currents vary slowly with temperature; any dependence that is observed is thought to be caused by the slow variation in bandgap energy with temperature.

3. Results

The first diode structures to be thoroughly characterized before and after postanneal were output diodes from the SP and LP pixel strings on samples from CIM Lot 24, the second lot to incorporate the CIMTEK photomask design and ASP. The leakage current density for one of these diodes, 24-2-BU-SPA, as a function of inverse temperature before and after postanneal, for a junction reverse bias of 0.4 V, is shown in Figure 3-5. The device was baked for 15 hours at 100°C. During all I-V measurements, the common field plate and single-pixel transfer gates are biased to minimize the leakage current and the effects of guard-ring field-induced junctions. The dashed line in the figure shows the theoretical slope for a diffusion-dominated leakage mechanism. The measured IR cutoff for this sample (at 77 K) was 8.9 μm.

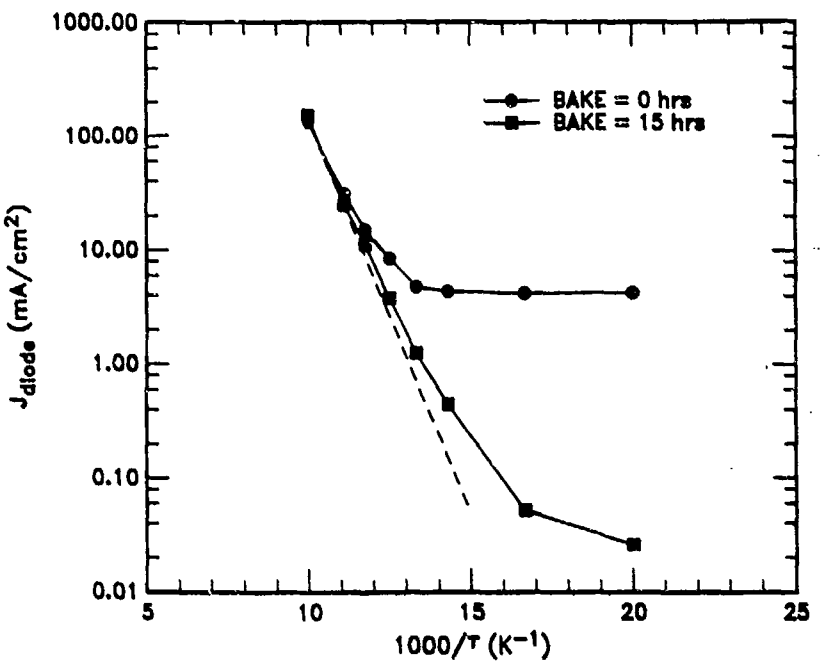


Figure 3-5. Leakage current density for diode 24-2-BU-SPA as a function of inverse temperature before and after baking at 100°C, for a junction reverse bias of 0.4 V. The dashed line shows the theoretical slope for a diffusion-dominated leakage mechanism.

Before postanneal, the leakage current density is invariant with temperature below 80 K (1000/T = 12.5), indicating a tunneling-dominated leakage mechanism. After postanneal, the tunneling component is greatly reduced in magnitude and does not dominate the temperature behavior even at 50 K. Under these bias conditions, the diode appears to be diffusion-limited down to about 75 K (1000/T = 13.3). Figure 3-6 shows the corresponding data for junction biases ranging from 0.05 V to 0.8 V. As the bias is increased, the reduction in tunneling current with baking becomes more pronounced, and is better than two orders of magnitude for 0.8 V reverse bias. For 0.05-V bias, the diode appears to be diffusion-limited down to 50 K after postanneal. The leakage current density at 80 K and 0.1-V reverse bias was 3.5 mA/cm^2.

Although diode tunneling currents are significantly reduced after postanneal, the diffusion dark current is slightly increased, as evidenced by the data points in the region of 80 K and above. (This is probably an indication that the bulk minority-carrier lifetime degraded somewhat with baking.) For detectors operated at 70 K or below, the important effect will be the significant reduction in tunneling dark current, which will allow the use of higher diode reset potentials with little or no attendant increase in leakage currents and associated shot noise.

These first results were confirmed by measurements on devices from CIM Lot 26, also a CIMTEK lot with ASP. Results for diode 26-2-BU-SPB before and after a 24-hour/100°C postanneal are shown in Figure 3-7 for junction reverse biases of 0.1, 0.4, and 0.8 V. The corresponding pre- and post-bake I-V characteristics at 77 K are shown in Figure 3-8. At 0.1-V bias, the leakage current is tunnel-limited below 65 K before bake; after bake, the tunneling component is not completely dominant even at 50 K, and the current appears diffusion-limited down to about 60 K. At 0.4 V, the reduction in tunneling current is greater than two orders of magnitude, and the diode leakage remains diffusion-limited above 65 K after bake. At 0.8 V, the improvement on baking is not as dramatic but is still better than an order of magnitude, and leakage current is still diffusion-limited at 77 K. The post-bake leakage current at 77 K [Figure 3-8(b)] varies by only a factor of 2 between 0.1 V and 0.8 V reverse bias. Results for the companion BU output diode were nearly identical to these.

Another Lot-26 device, 26-2-BU-LP (a large-pixel string), was subjected first to the standard 24-hour postanneal and then to an additional 51 hours at 100°C. I-V characteristics for the two adjacent diodes are shown in Figure 3-9 at the three stages of annealing. In both cases, the additional 51-hour bake produced a further reduction in leakage at all bias levels, even below 100 mV (where a 24-hour bake sometimes produces a small increase. Final leakage-current densities at 0.5 V were as low as 2.8 mA/cm^2, the lowest value observed at 77 K on an LP diode (with total area about five times that of an 8 × 8 CIM column diode). The corresponding CIMs could be operated at 0.5-V reverse bias with only a 20% increase in diode leakage over the value at 0.1 V.

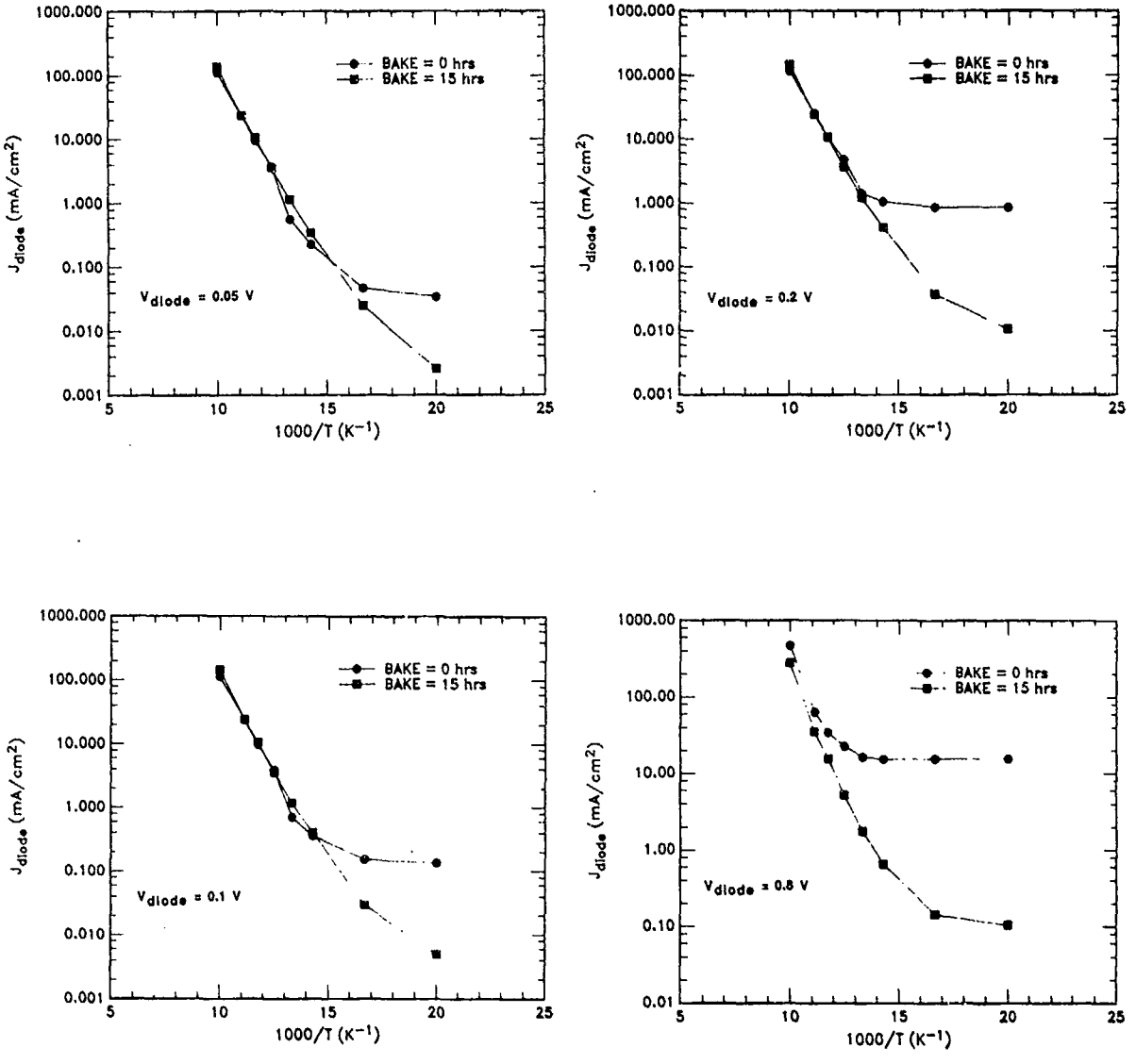


Figure 3-6. **Leakage current density for the diode of Figure 3-5 as a function of inverse temperature before and after bake, for four different junction reverse biases.**

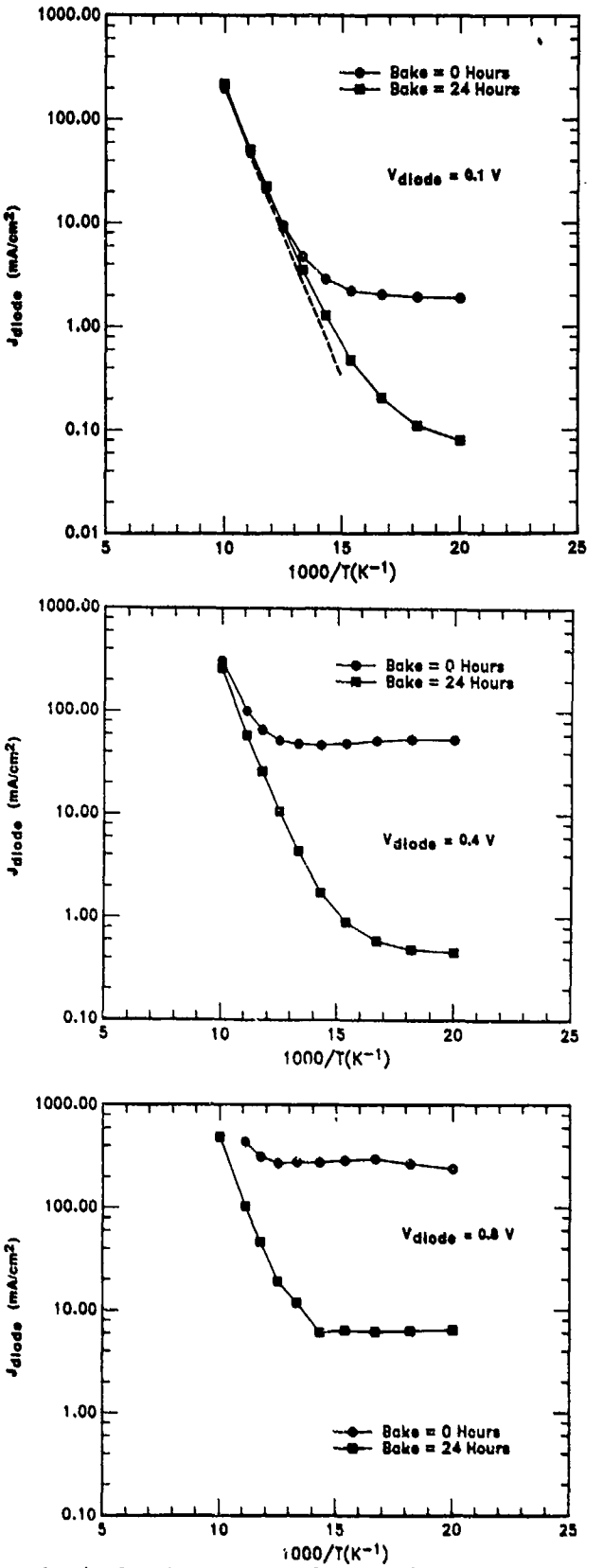


Figure 3-7. Leakage current density for diode 26-2-BU-SPB as a function of inverse temperature before and after baking at 100°C for three different junction reverse biases. Dashed line in upper figure is for a diffusion-dominated leakage mechanism.

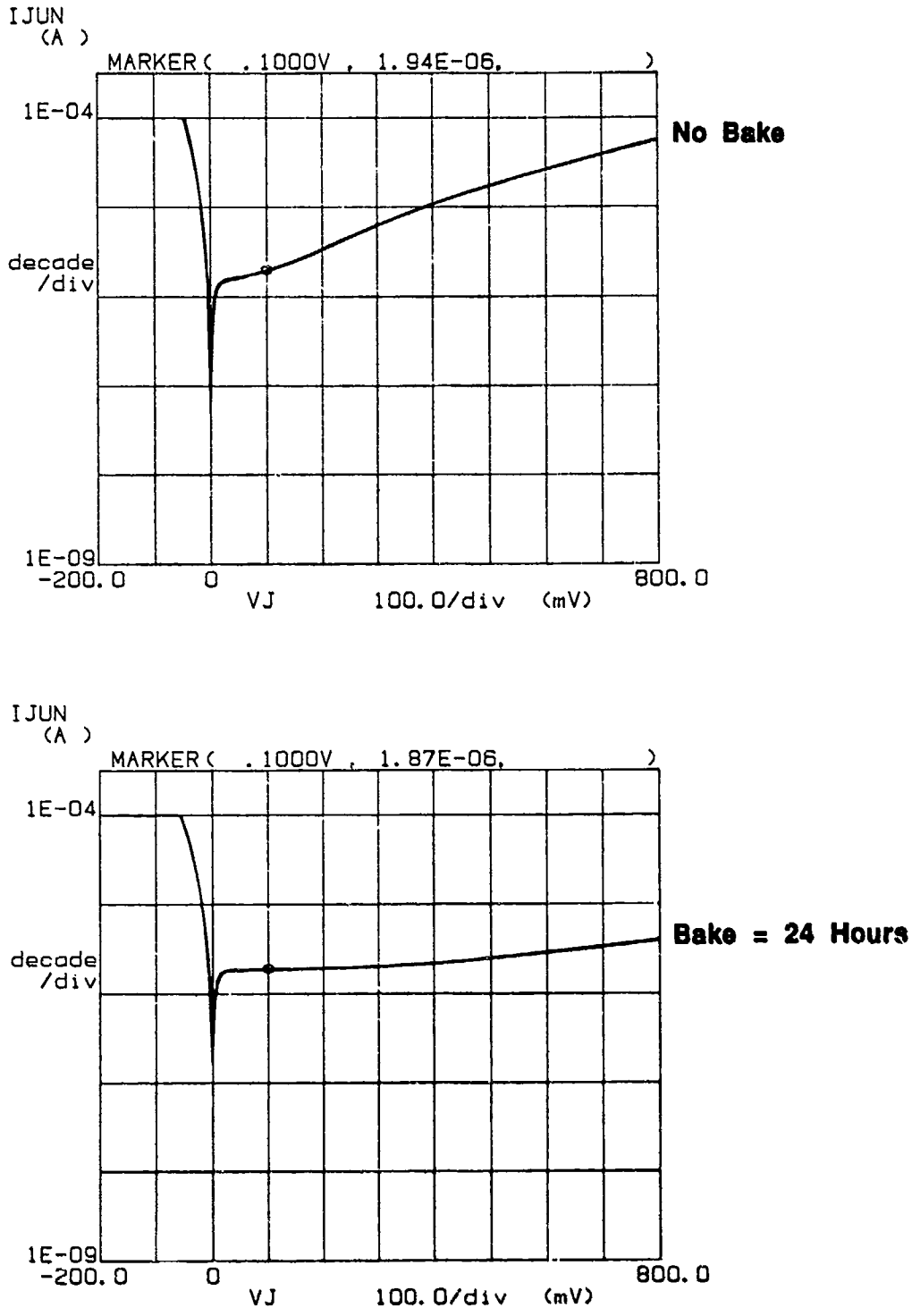


Figure 3-8. Current-voltage characteristics of diode 26-2-BU-SPB at 77 K and 0-degree FOV, before (upper plot) and after (lower plot) 100°C postanneal. Marker is at 0.1 V reverse bias in each case.

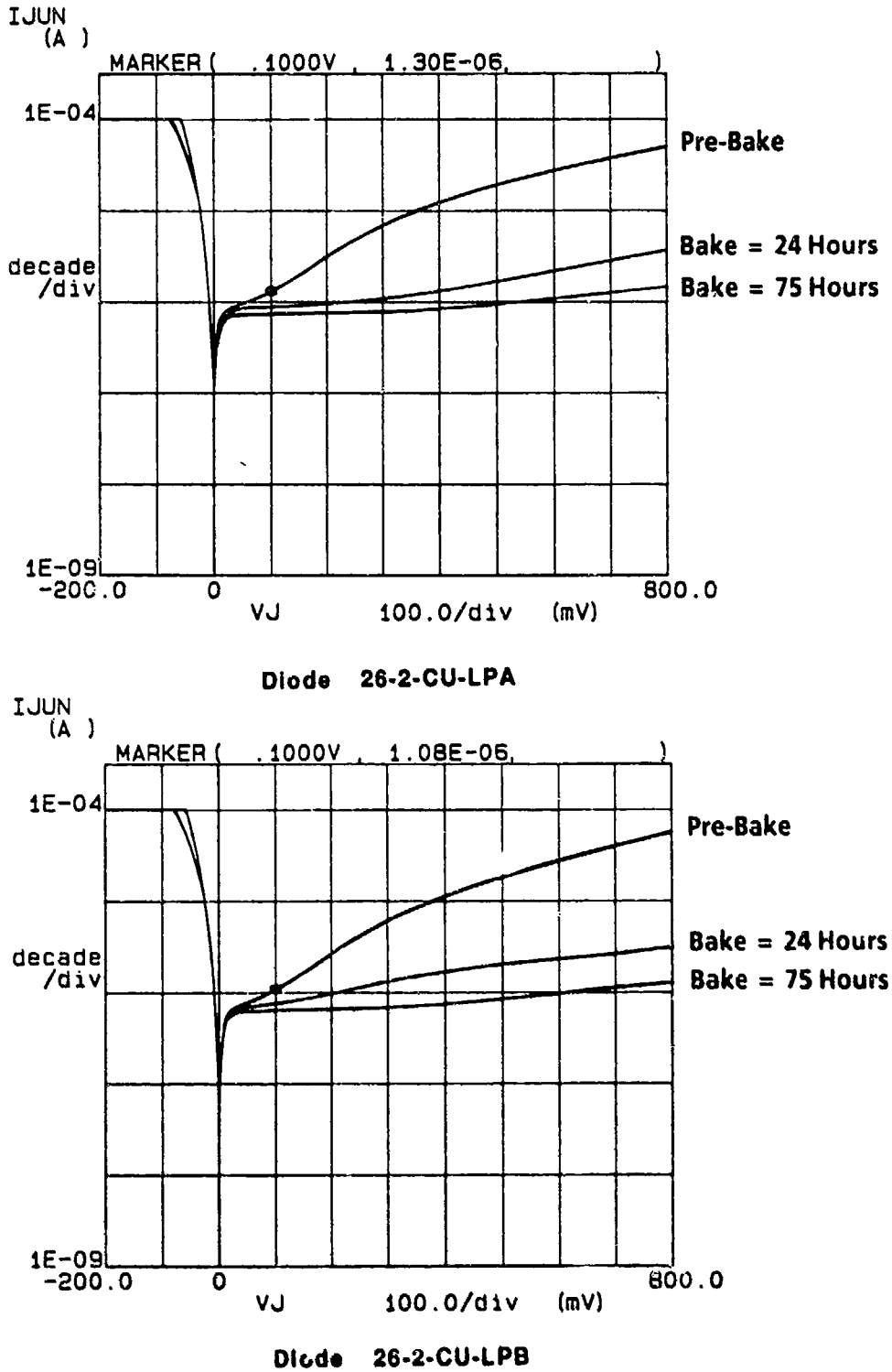


Figure 3-9. Current-voltage characteristics at 77 K and 0-degree FOV at three stages of postannealing, for neighboring diodes 26-2-CU-LPA (upper plot) and 26-2-CU-LPB (lower plot). Marker is at 0.1-V reverse bias on the prebake curves.

Plots of leakage current versus inverse temperature for one of these LP diodes are shown in Figure 3-10. Only the single measurement at 77 K was made following the additional 51-hour bake. Although data were not taken as a function of temperature for this last case, it is expected that the onset of tunneling behavior has moved to even lower temperatures (<60 K) following the additional anneal. As in the case of the other Lot-26 device, results for the companion CU-LP diode were virtually identical.

A counterexample to this behavior was provided by the first Lot-24 device tested. Results for one diode (24-2-BU-SPA) on this device are presented in Figures 3-5 and 3-6. The companion diode (24-BU-SPB), also baked for 15 hours at 100°C, showed significant degradation in tunneling current, as shown in Figure 3-11; diffusion currents also increased. This result is attributed to the high level of crystalline substructure present in some of the p-type substrates used in these earlier CIM lots. Speculation is that the junction area of the SPB diode may contain one or more isolated microstructural defects that cause degradation of diode character on baking. A direct correlation between microstructure and diode quality was demonstrated for large-area CIM staring arrays fabricated on MWIR LPE HgCdTe under Contract N00014-86-C-2193.[12] Microstructure could also explain the relatively high diffusion dark currents at 80 K (3.5 mA/cm^2) observed on both Lot-24 devices before and after bake: these can probably be attributed to lower-than-normal bulk minority-carrier lifetimes caused by higher-than-normal substrate defect densities.

The facts that, in most cases, neighboring diodes exhibit nearly the same I-V characteristics and that these change in nearly identical fashion on postannealing suggest that the HgCdTe substrate in these cases is relatively free of microstructural defects, at least in the regions occupied by the test structures studied. A detailed investigation of the effects of crystalline substructure on both diode and MIS performance was beyond the scope of this program. However, all substrate material used for subsequent IRST array fabrication was carefully prescreened for microstructure (using a proprietary defect-etch procedure), as discussed in Section IV.C, and only samples having sufficiently low defect densities were retained.

D. DIODE 1/f NOISE

To investigate the mechanisms of 1/f noise in ion-implanted diodes, a series of measurements was performed using structures from a specially designed diode test bar fabricated under IR&D funds. All measurements and data analysis reported here were performed under the present contract.

All diode structures were fabricated with anodic-sulfide passivation using the standard CIM boron implantation process, and all incorporated upper-level guard rings that serve the same function as the CIM field plate. Before testing, all structures were postannealed at 100°C (under room ambient) for 200 hours to simulate the effects of a typical dewar bake-out cycle. Structures included diodes of fixed area (5.6×10^{-4} cm^2) but varying perimeter-to-area (P/A) ratio to permit the study

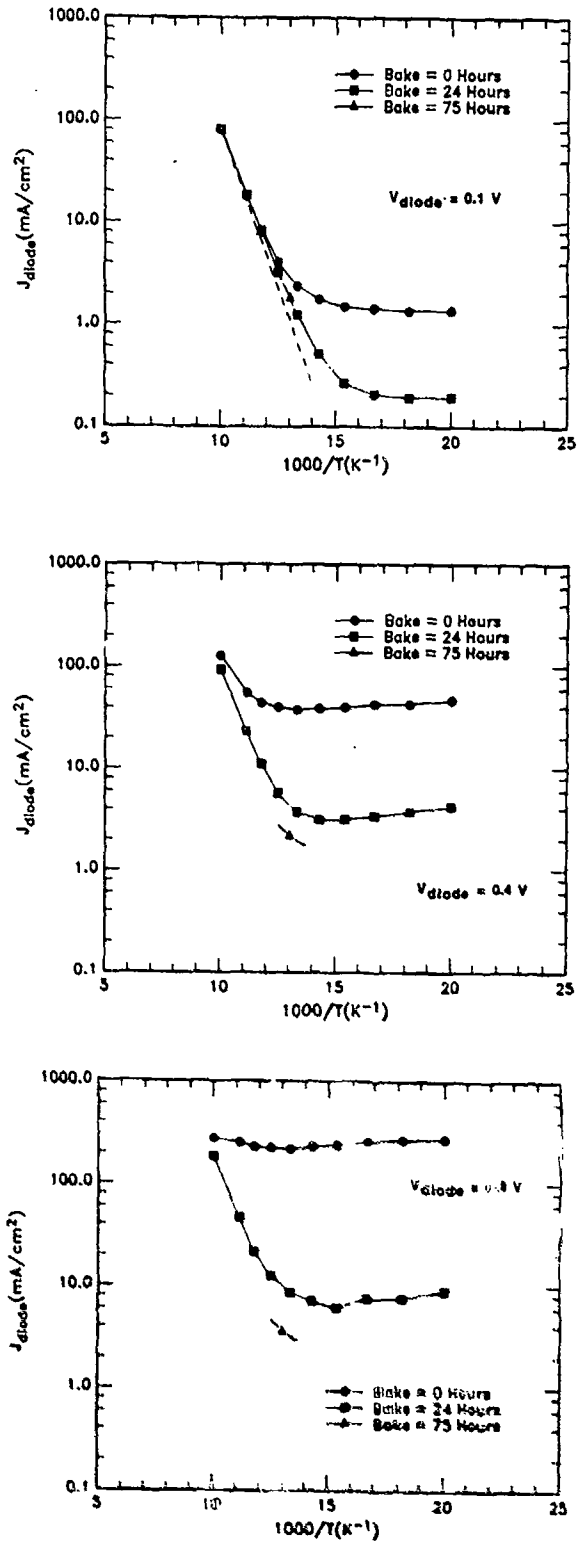


Figure 3-10. Leakage current density for diode 26-2-3U-LPB as function of inverse temperature at three stages of postannealing for three reverse-bias levels. Measurements following final bake (75 hours) were made at 77 K only. Dashed line in upper figure is for diffusion-dominated leakage mechanism.

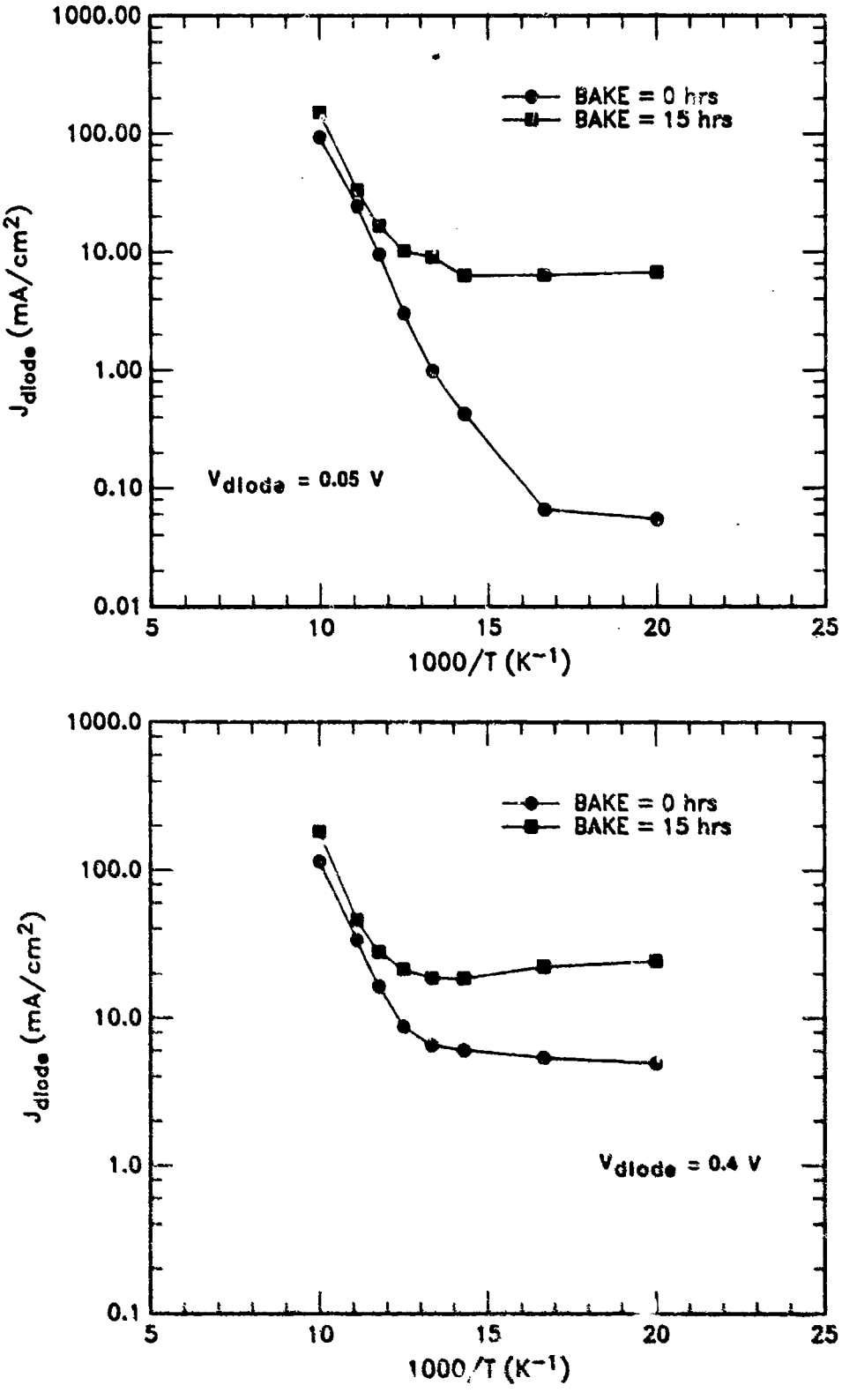


Figure 3-11. Leakage current density for diode 24-3-BU-SPB before and after postanneal, for reverse biases of 0.05 V and 0.4 V. Compare with Figures 3-5 and 3-6.

of surface effects as well as to simulate the high aspect ratios of typical CIM diodes. Substrate material in all cases was solid-state-recrystallized HgCdTe of 9.8-μm cutoff.

Diode noise currents were measured directly using an HP-3562A Dynamic Signal Analyzer. Both dark current and noise current were measured as a function of temperature to investigate the physical mechanisms involved in each. Typical results are shown in Figure 3-12. The plotted noise current in the figure is the spectral noise density (spot noise) at a frequency of 2 Hz and is a measure of the diode l/f noise. As with the leakage-current measurements reported in Subsection III.C, two distinct regions are observed. The dark current at low temperatures again is consistent with tunneling-dominated behavior, and at high temperatures follows a $1/n_i^2$ slope (also shown in the figure), characteristic of diffusion-limited behavior.

The low-frequency noise current at low temperature exhibits a similar insensitivity to temperature, suggesting a tunneling mechanism as the dominant low-temperature noise source. This conclusion is supported also by the dependence of noise current on guard ring bias, as discussed later. At higher temperatures, the noise current follows a $1/n_i$ slope, which does not clearly establish the noise-current mechanism. The $1/n_i$ slope is characteristic of depletion g-r-limited behavior in diode dark current; however, an independent analysis by Kleinpenning[13] has predicted a direct dependence of low-frequency noise current on the square root of diode diffusion current, which would vary as $1/n_i$.

To resolve this question, both noise and dark current were measured on four proximate diodes having equal areas but different perimeters. Measurements were performed at 100 K, where all diodes were clearly diffusion-limited. Results are shown in Figure 3-13. No correlation is evident between the diffusion dark current and low-frequency noise current.

To establish the spatial origin of the high-temperature component of noise current, the 100 K noise measurements on these same four diodes were plotted versus P/A ratio, as shown in Figure 3-14. A clear dependence of noise current on perimeter is seen, suggesting the surface region as the origin of low-frequency noise current at high temperatures. This result is consistent with surface g-r as the source of low-frequency diode noise current.

A correlation between surface g-r current and noise current has previously been noted by Tobin et al.[14] and Chung et al.[15] for MWIR ion-implanted diodes passivated with ZnS, by Radford et al.[16] for MWIR ion-implanted and double-epilayer diodes passivated with SiO_2, and by Briggs et al.[17] for LWIR ZnS-passivated diodes. The present study suggests a similar result for LWIR ion-implanted diodes passivated with anodic sulfide. It differs in that in no temperature regime is the diode dark current dominated by surface g-r effects. However, both Tobin et al. and Radford et al. found temperature regimes where diode dark current was diffusion-limited but diode noise current was surface g-r-limited.

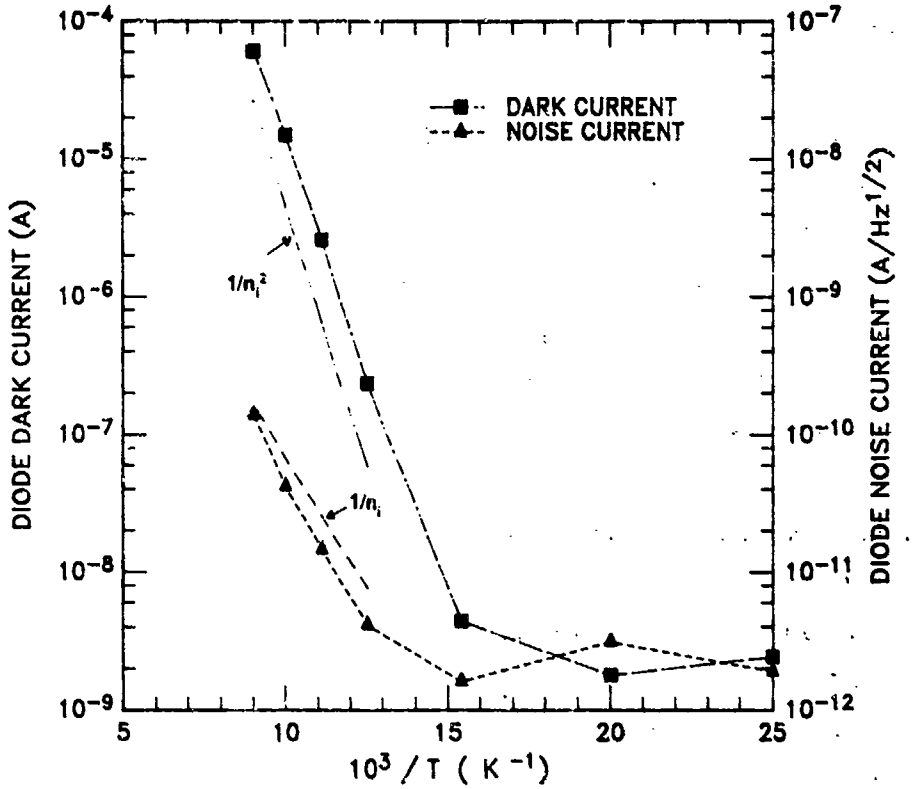


Figure 3-12. Temperature dependence of diode leakage current and noise-current spectral density (f = 2 Hz) for junction reverse bias of 0.25 V. Detector cutoff 9.8 μm.

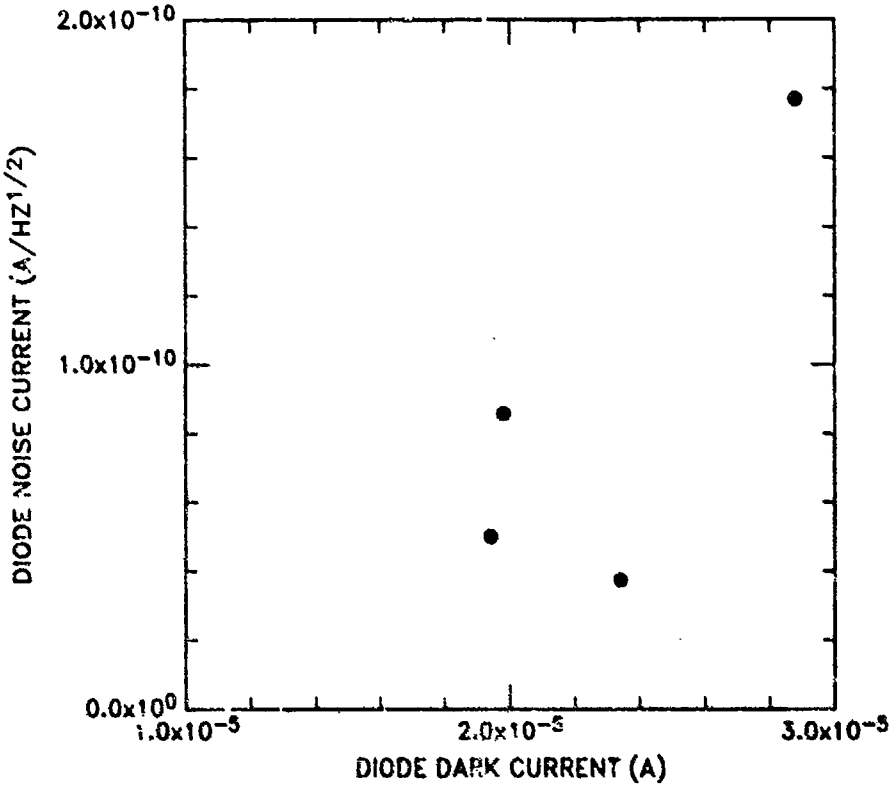


Figure 3-13. Correlation of diode dark current to diode noise current (f = 2 Hz) for four different diodes at 0.25-V reverse bias at temperature of 100 K. Dectector cutoff = 9.8 μm for all cases.

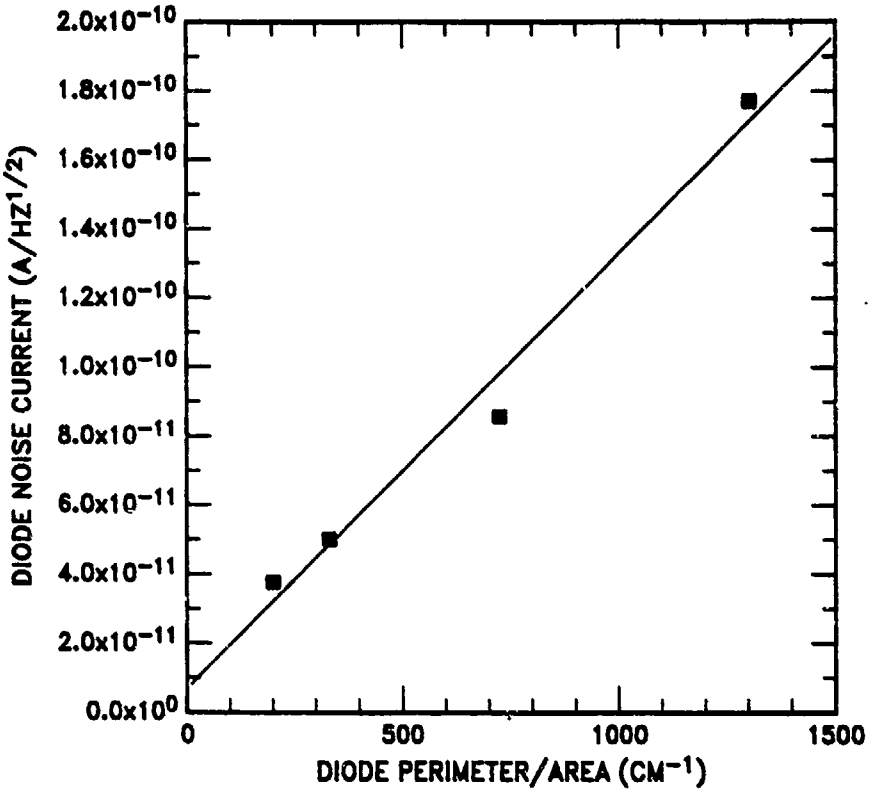


Figure 3-14. Correlation of diode noise current (f = 2 Hz) to diode perimeter/area ratio at 100 K for same four devices as in Figure 3-13.

The absence of a measured diode dark current caused by surface g-r prevents a quantitative comparison of these results with the theory relating diode noise current to surface g-r current for the case of surface-potential fluctuations[18] or bremsstrahlung.[16] However, past studies showed the proportionality constant between surface g-r current and noise current to be about 10^{-3} to 10^{-4} (though for different surface passivations and bandgaps). Using the same constant for the present case yields a surface g-r current much smaller than the measured diffusion current.

The sensitivity of diode dark current to guard-ring bias is also of interest. In the tests described previously, guard rings were biased to minimize diode leakage current. Here, the guard-ring bias is varied while diode dark and noise currents are measured.

Figure 3-15 illustrates the high-temperature (100 K) results. At large negative guard-ring bias, a field-induced junction is formed under the gate over the n-side of the diode. This junction is highly doped on both sides since it lies between a heavily accumulated p^+ region and the more highly doped n^+ regions. This enhances the probability of tunneling, producing an exponential dependence of dark current on gate bias. The noise current is similarly affected. At more positive guard-ring biases, a depletion (and ultimately an inversion) region forms under the guard-ring gate on the p-side. Since this does not significantly affect the diffusion volume, little change occurs in the diode dark

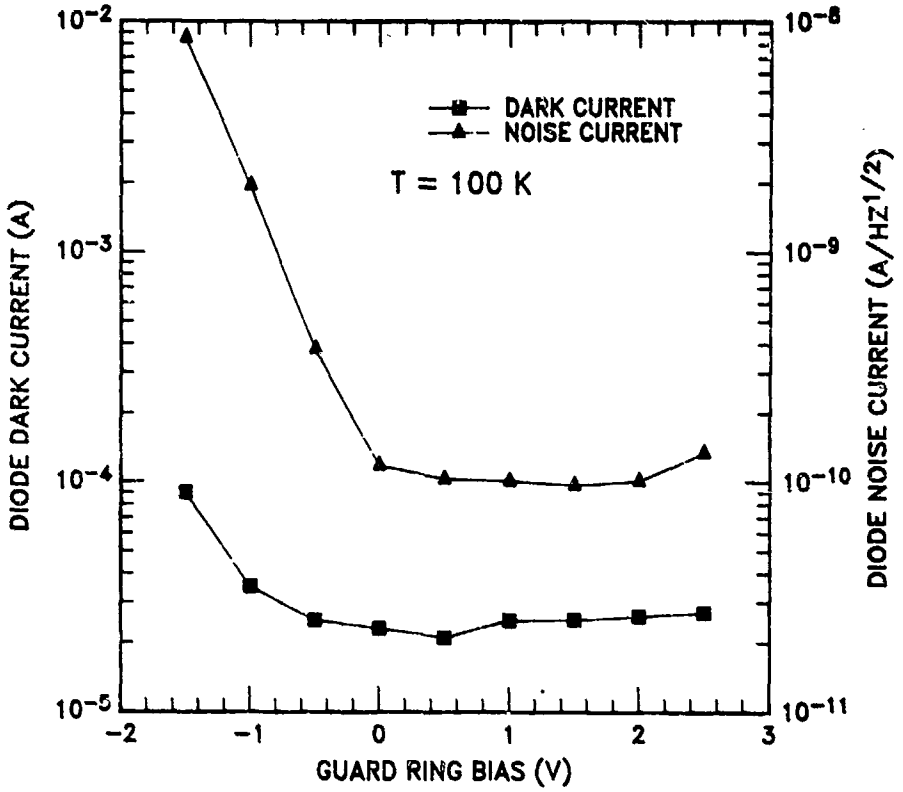


Figure 3-15. Gate-bias dependence of diode dark current and diode noise current (f = 2 Hz) at 0.5-V junction reverse bias and T = 100 K. Detector cutoff = 9.8 μm.

current. The increased surface depletion-region area should increase the surface g-r current, however, and a small rise in diode noise current is noted at about +1 V bias.

Figure 3-16 presents the low-temperature (40 K) results. At low gate biases, the field-induced junction on the n-side affects both dark and noise currents in a manner similar to the high-temperature case. At higher gate biases, the field-induced junction on the p-side tunnels sooner than at 100 K (since the bandgap is smaller at 40 K), and tunneling produces an exponential rise of dark and noise currents with increasing gate bias. The net effect is an overall increased sensitivity of diode noise and dark currents to guard-ring bias compared with higher temperatures.

Comparison of the curves in Figure 3-16 shows that the diode noise current is more sharply sensitive to gate bias, while the diode dark current exhibits a relatively bias-insensitive region about 1.5 V wide. This suggests that the diode noise current may be caused exclusively by surface tunneling effects while, in the same range of gate biases, the diode dark current is limited by tunneling in the bulk.

In conclusion, the low-frequency diode noise current in ASP ion-implanted LWIR diodes appears to be caused by surface g-r currents for temperatures greater than about 80 K and by tunneling (chiefly surface) effects for temperatures less than about 80 K. In addition, the noise current at lower

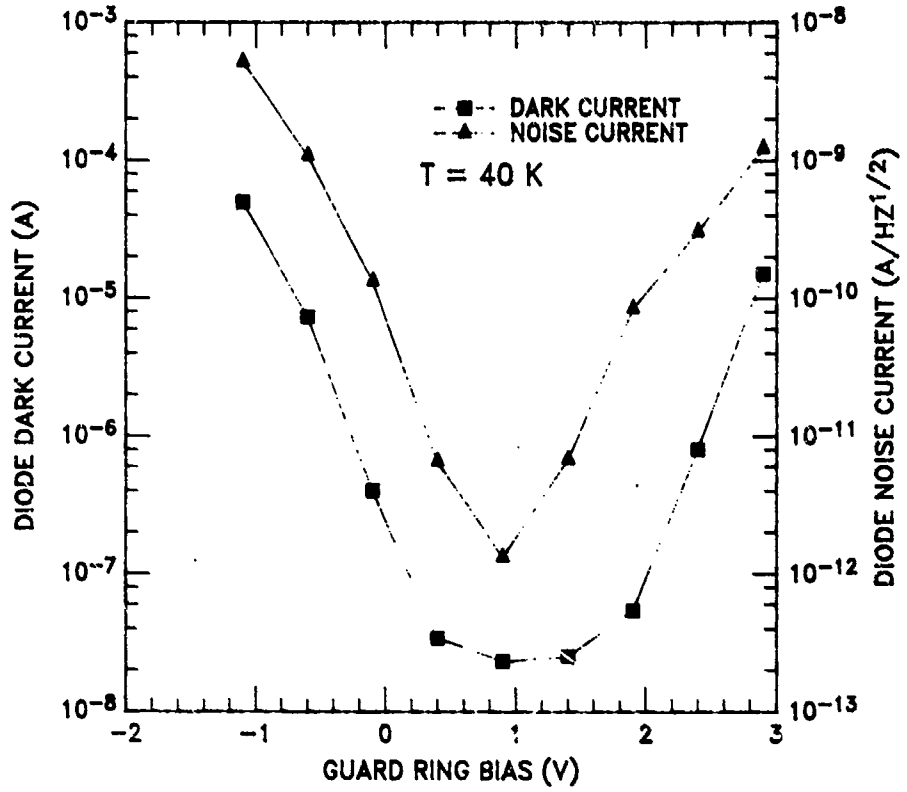


Figure 3-16. Gate-bias dependence of diode dark current and diode noise current (f = 2 Hz) at 0.5-V junction reverse bias and T = 40 K. Detector cutoff = 9.8 μm.

temperatures is more sensitive to guard-ring bias because of enhanced tunneling through the field-induced junction on the p-side. These results agree qualitatively with previous studies employing different surface passivations and bandgaps.

E. HgCdTe SUBSTRATE THINNING

A key technology issue for the VICIM array structure is the ability to thin p-type HgCdTe to substrate thicknesses of about 10 to 20 μm without degradation of MIS properties. To demonstrate this capability, experiments were conducted using standard MIS test structures commonly employed for materials characterization and surplus p-type HgCdTe substrates of 9- to 10-μm cutoff wavelength. Material selected had generally low substructure and defect density, but was deemed unsuitable for array fabrication because of isolated surface defects or substructure nonuniformity.

To the extent that MIS dark currents are diffusion-limited, substrate thinning may be expected to enhance MIS character by reducing the available diffusion volume beneath the detector gates, thereby reducing the total dark current and increasing MIS storage times. This effect can be modeled as a function of both temperature and substrate thickness, and results of a typical calculation are illustrated in Figure 3-17. The model assumes a net acceptor concentration of 1×10^{15} cm^{-3}, a minority-carrier lifetime of 1 μs, (for both bulk and thinned samples), a bias past

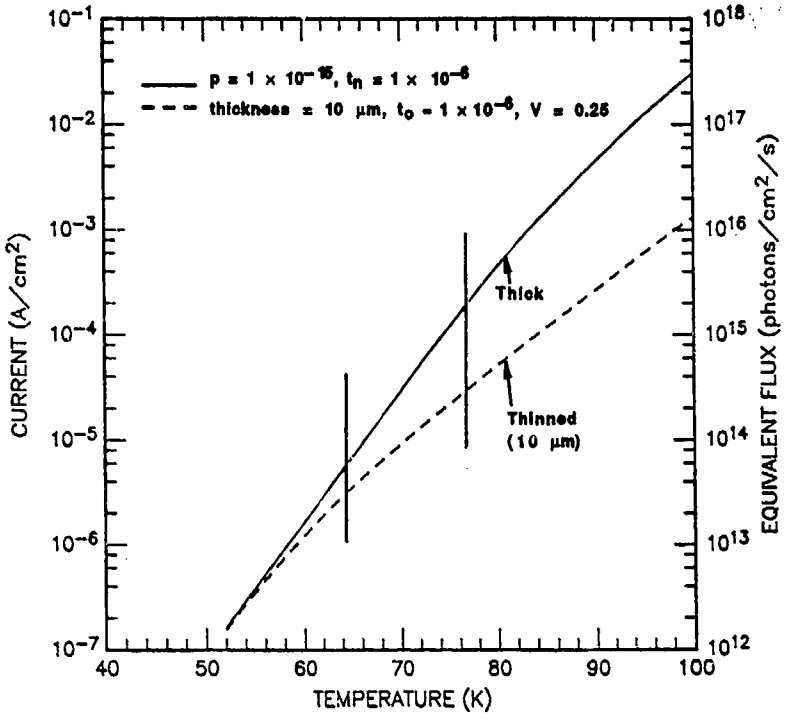


Figure 3-17. Model calculation of MIS dark-current density versus temperature for unthinned (bulk) and thinned (10-μm thickness) p-type HgCdTe of 10 μm cutoff. Vertical markers are at 65 K and 77 K. The calculation for thinned substrate assumes an accumulated back surface.

threshold of 0.25 V, and a cutoff wavelength of 10 μm. It is also assumed that the back surface of the thinned substrate is maintained in accumulation, either by a suitable backside passivation or by a bias-controlled backside gate, so that the back surface does not act as an uncontrolled source of excess minority carriers. Diffusion lengths in device-grade LWIR p-type HgCdTe are sufficiently long (typically several mils or more) that an inverted back surface could cause severe degradation of MIS properties in thinned samples.[19]

As the figure shows, the model predicts a significant reduction (nearly an order of magnitude) in MIS dark current at 77 K for a substrate thinned to 10 μm. At lower temperatures, the improvement is increasingly less significant as the diffusion current becomes progressively less dominant. At 65 K, the reduction is only a factor of 2; however, at this lower temperature, the dark current for both bulk and thinned samples is about an order of magnitude lower than at 77 K. These results suggest that optimum MIS performance could be obtained by operating a suitably thinned and passivated HgCdTe substrate at temperatures approaching 60 K.

To confirm this expectation, a series of experiments was performed using material selected on the basis of combined Hall measurements and defect-etch data. All samples were core-annihilated

material having p-type Hall characteristics and fairly uniform crystalline microstructure with low dislocation densities. The standard experimental outline was as follows:

1. Divide substrate into four segments of roughly equal area.
2. Flatten, polish, and passivate back surfaces and mount to carriers.
3. (a) Control sample: Standard frontside prep and passivation.

   (b) Other three samples: Thin to 30 μm, 20 μm, and 10 μm final thickness and passivate.
4. Fabricate standard MIS test structures (5 × 40 mil transparent and opaque gates with guard rings) on all samples.
5. Evaluate.
6. Postanneal for 20 to 30 hours at 100°C and reevaluate.

The first series of experiments was inconclusive. Results for the four samples from a typical substrate are shown in Table 3-3. In this example, only the control sample and the sample thinned to 10 μm evidenced p-type C-V character, and postannealing at 100°C failed to produce any improvement; the best MIS storage times observed were 5 μs. The samples thinned to 30 μm and 20 μm tended to n-type character (one before and one after postanneal), with no measurable MIS storage in either case. Samples from other substrates exhibited similar inconsistencies in MIS data, and it was concluded either that the MIS quality of the original starting material was inadequate to permit meaningful determination of the effects of substrate thinning, or that the thinning procedures and subsequent device processing were inconsistent.

Table 3-3. Thinned p-Type MIS Results

Sample	Material ID	Thickness (μm)	Postanneal	C-V Character (1 MHz; 77 K)	Dark Storage Time (μs)
3-A	1007-48	Unthinned	None	Marginal p-type	4–5
			64 hrs/100°C	Marginal p-type	<5
3-B	1007-48	30	None	Low-frequency	0
			64 hrs/100°C	Poor n-type	0
3-C	1007-48	20	None	Marginal n-type	0
			64 hrs/100°C	Low-frequency	0
3-D	1007-48	10	None	Marginal p-type	2-3
			64 hrs/100°C	Low-frequency	0

A concurrent series of experiments performed under internal funding was more conclusive, however, and we include these results here since they are significant to the ongoing VICIM development effort. Figure 3-18 shows the results of MIS storage-time measurements at 77 K on seven p-type SSR samples with measured IR cutoffs ranging from 8.5 to 9.5 μm. All samples were thinned to 10 μm (with no unthinned control sample) and backside-passivated, and all were postannealed following test-structure fabrication. Average dark-storage times ranged from 200 μs at 9.4 μm cutoff to greater than 1 ms at 8.5 μm cutoff. For comparison, the figure also shows the storage-time trend line for device-grade unthinned n-type SSR material at 77 K. In all cases, the thinned p-type samples exhibit superior MIS performance.

These initial experiments have now been repeated several times with largely consistent results, and further experiments and analysis are being conducted on internal funding. Figure 3-19 shows full-well and half-well storage-time data at 77 K for two halves of a p-type SSR sample, one half thinned to 10 μm and processed in standard fashion, the other (control) half left unthinned. Measured IR cutoff was 10.0 μm. Storage times ranged from 25 μs to 165 μs for the thinned sample and from 5 μs to 45 μs for the unthinned sample. (Data in the figure are arranged in ascending order for the 14 test capacitors measured.) In all cases, the enhancement in storage time on thinning was at least a factor of 3.5, and the enhancement in half-well storage time was about a factor of 2. (The half-well storage time provides a more meaningful measure of the charge integration capacity of the MIS structure and is now a standard figure of merit in MIS material evaluations.)

These results are not isolated but are typical. Approximately three-fourths of all p-type substrates evaluated in this fashion have shown similar results. Although further testing and analysis are required to understand these effects in detail (in particular, why the same results are not obtained in every case), the work thus far provides strong evidence that MIS performance can be preserved and enhanced by thinning of p-type substrates to the thicknesses required for the VICIM fabrication process.

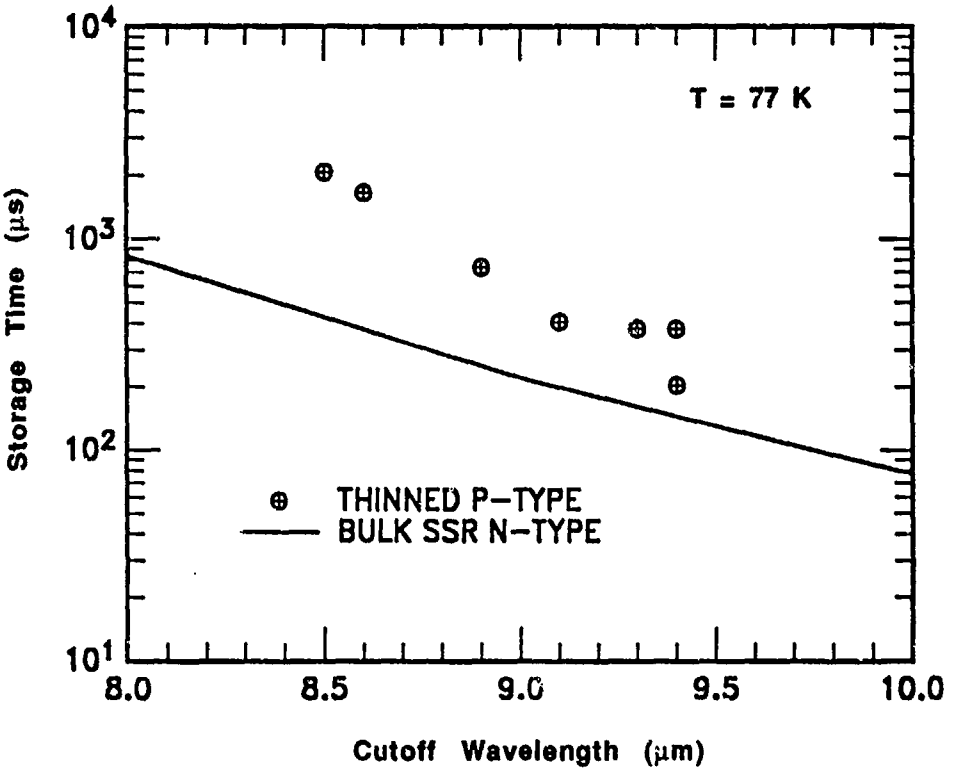


Figure 3-18. Average MIS dark-storage times on seven thinned p-type SSR HgCdTe substrates (all 10-μm thick) as function of measured IR cutoff at T = 77 K. Solid curve is empirical trend line for device-grade bulk SSR n-type HgCdTe at 77 K.

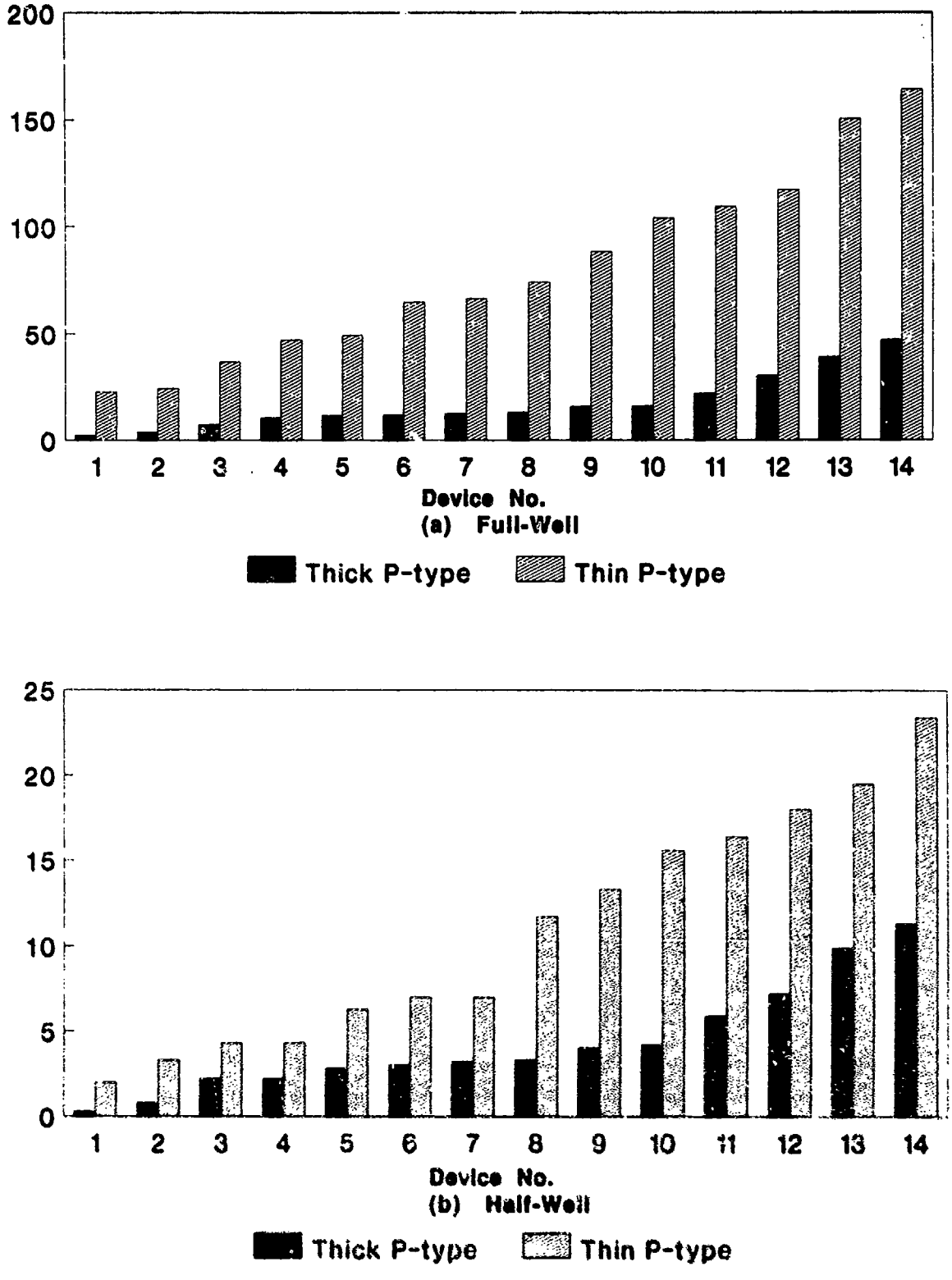


Figure 3-19. Full-well and half-well MIS dark-storage times (μs) at 77 K for two halves of same p-type HgCdTe substrate. One half was thinned to 10 μm thickness (shaded bars) and other half was left unthinned (solid bars) for comparison. Data for 14 gates arranged in ascending order of storage time. Measured IR cutoff was 10.0 μm.

SECTION IV
CIM PROCESS DEVELOPMENT AND ARRAY FABRICATION

The fabrication process used for both the CIMTEK technology-development lots and the IRST array lots was a development of the baseline CIM process used on the previous 64 × 120 CIM array program[20] (NRL Contract N00014-84-C-2062), and incorporated a number of process advances developed under the concurrent Large-Area (128 × 128) CIM array program[21] (NRL Contract N00014-86-C-2193). The goal of the processing effort was twofold: first, to identify and eliminate principal yield-loss mechanisms associated with the baseline CIM process; and second, to ensure compatibility of the optimum CIM process with the added fabrication requirements of the vertically integrated CIM structure.

Advanced CIM process development was beyond the defined scope of the present program and was supported on internal funding. The essential results of this effort and their impact on IRST array yields and producibility are reported here for completeness.

A. STANDARD PROCESS FLOW AND YIELD-LOSS MECHANISMS

The standard CIM fabrication process as implemented at the outset of the program is outlined in Table 4-1 and incorporates a total of 14 photomask steps. All metal gate levels, with the exception of the MIS transparent gate (thin nickel), are aluminum, defined by a negative-photoresist liftoff process; the bus-metal fuse is thin evaporated Ni, and the bond metal is a Pb-In composite. The gate insulator is ZnS deposited by MOCVD, and the interlevel insulator is evaporated ZnS. Surface passivation is the current standard anodic sulfide process (ASP) for long-term thermal stability, especially in p-type MIS detector structures.

The fabrication process flow for the vertically integrated CIM (VICIM) structure is outlined in Table 4-2 and illustrated schematically in Figure 4-1. The HgCdTe substrate is first backside-passivated and epoxied to a prescreened silicon processor, then thinned to a final operating thickness of 8 to 12 μm. Interconnect vias are etched through the HgCdTe to the underlying Si input nodes. The standard monolithic CIM fabrication process follows, followed by final etching of the Si vias and deposition of interconnect metal. Three additional photomask levels are required (beyond the 14 of the standard CIM process) to achieve the VICIM structure.

Equivalent via-formation and interconnect process technologies have been demonstrated successfully with several recent prototype focal planes, notably the Advanced Antitank Weapon System—Medium (AAWS–M) 64 × 64 staring array family[22] and the Advanced Scanning Array Module (ASAM–II) 960 × 1 scanning array[23] for FLIR. While the AAWS–M arrays feature direct interconnection to Si at each pixel site, the ASAM-II and infrared search/track (IRST) scanning

Table 4-1. Baseline CIM Process Flow

	Process Step	Photomask No.
1.	Material selection	
2.	Thinning and surface preparation	
3.	Passivation (ASP)	
4.	Gate insulator deposition (MOCVD ZnS)	
5.	Diode pattern and implant	1
6.	MIS thin gate definition	2
7.	Diode contact definition	3
8.	MIS opaque gate definition	4
9.	Second ZnS deposition	
10.	Field plate definition	5
11.	Field plate via-stop	6
12.	Third ZnS deposition	
13.	Transfer gate definition	7
14.	Final ZnS deposition	
15.	Transfer gate via	8
16.	Field plate via	9
17.	MIS gate via	10
18.	Scribeline etch	11
19.	Substrate via	12
20.	Bus metal fuse	13
21.	Bus metal interconnect	14
22.	Inspect and dc probe	

Table 4-2. VICIM Process Flow

1. Material selection
2. Backside polish and passivation
3. Epoxy to silicon processor
4. Thin to 8- to 12-μm thickness
5. Etch interconnect vias through HgCdTe to Si
6. Standard CIM process flow (Table 4-1, through step 20)
7. Etch final vias through ZnS to processor
8. Deposit interconnect metal
9. Inspect and probe

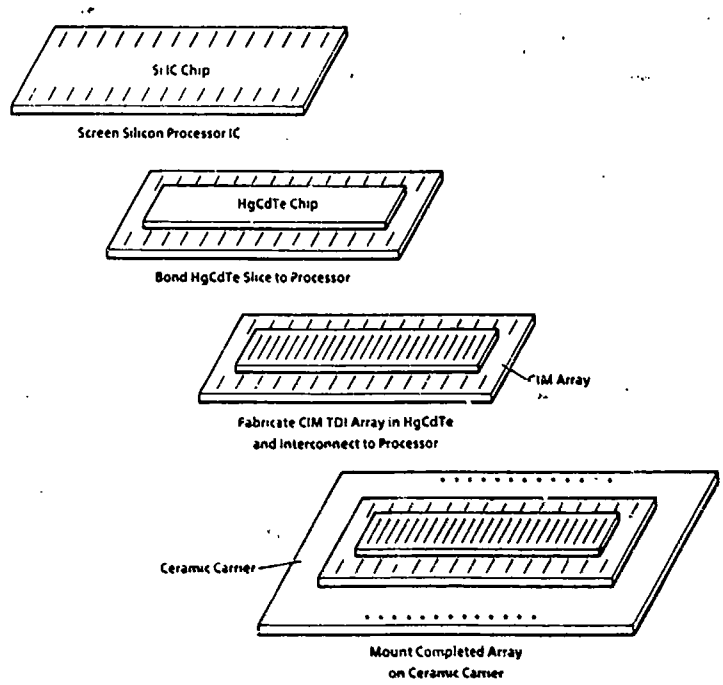


Figure 4-1. Schematic illustration of vertically integrated CIM (VICIM) fabrication process flow.

arrays are coupled at remote output nodes away from the active area of the detector. The latter design allows a greater tolerance margin on via sizing and also permits the use of somewhat thicker substrates since the vias can be larger than typical pixel geometries.

All IRST lots fabricated during the contract period were of the standard (nonvertically integrated) type. The first five lots processed were characterized by unacceptable fabrication yields. Room-temperature dc probe results for Lot 3A, summarized in Table 4-3, were typical. Detailed defect analysis, accomplished using a temperature-sensitive liquid-crystal probe technique,[21] revealed that the majority of electrical shorts were caused by interlevel (transfer gate and/or field plate to bus metal) defects, and the remainder caused by pinholes in the aluminum via-stop metal, which produced gate-to-substrate shorts.

These effects are illustrated schematically in Figure 4-2. The interlevel defects arise from "beading" of the upper-level metal electrode edges caused by the aluminum liftoff process. This effect was confirmed by SEM analysis of one Lot-3 array, as shown in Figure 4-3. The rough metal edges produce irregularities in the overlying insulator film that tend to propagate through subsequent layers and enhance the probability of interlevel shorts. The beading, clearly visible in the micrographs, provides direct visual evidence of the interlevel shorting mechanism. The other dominant defect, gate-to-substrate shorts arising from pinholes in the pixel via-stop, was confirmed by liquid-

Table 4-3. Probe Yield Summary for IRST Lot 3A

Array	Type	Substrate Material	Field Plate	Transfer Gate Left	Transfer Gate Right	Row Shorts to Substrate	Row Shorts to FP or TG	Net Row Yield (%)
3A-1	Linear	SSR	Intermittent short	Good	Short to substrate	4 of 8	4 or fewer	50
3A-3	Linear	SSR	Short to substrate	Short to substrate (or FP)	Short to substrate	8 of 8	8 of 8	0
3A-4	Linear	SSR	Short to substrate	Short to substrate (or FP)	Short to substrate	8 of 8	8 of 8	0
3A-5	Linear	SSR	Intermittent short	Short to substrate	Good	2 of 8	1 of 8; 1 high capacitance	63
3A-6	Linear	SSR	Good	Short to substrate	Short to substrate	7 of 8	0 of 8	13

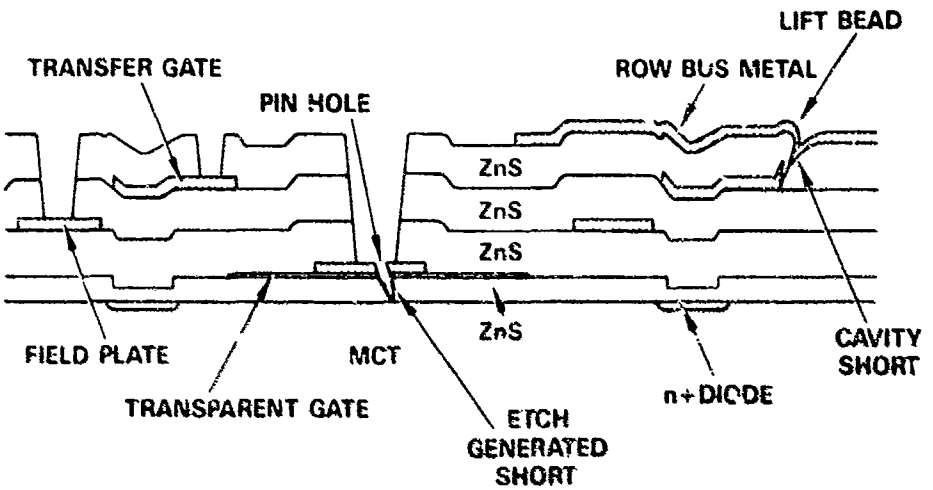


Figure 4-2. Schematic CIM cross section illustrating two principal yield-loss mechanisms associated with standard fabrication process.

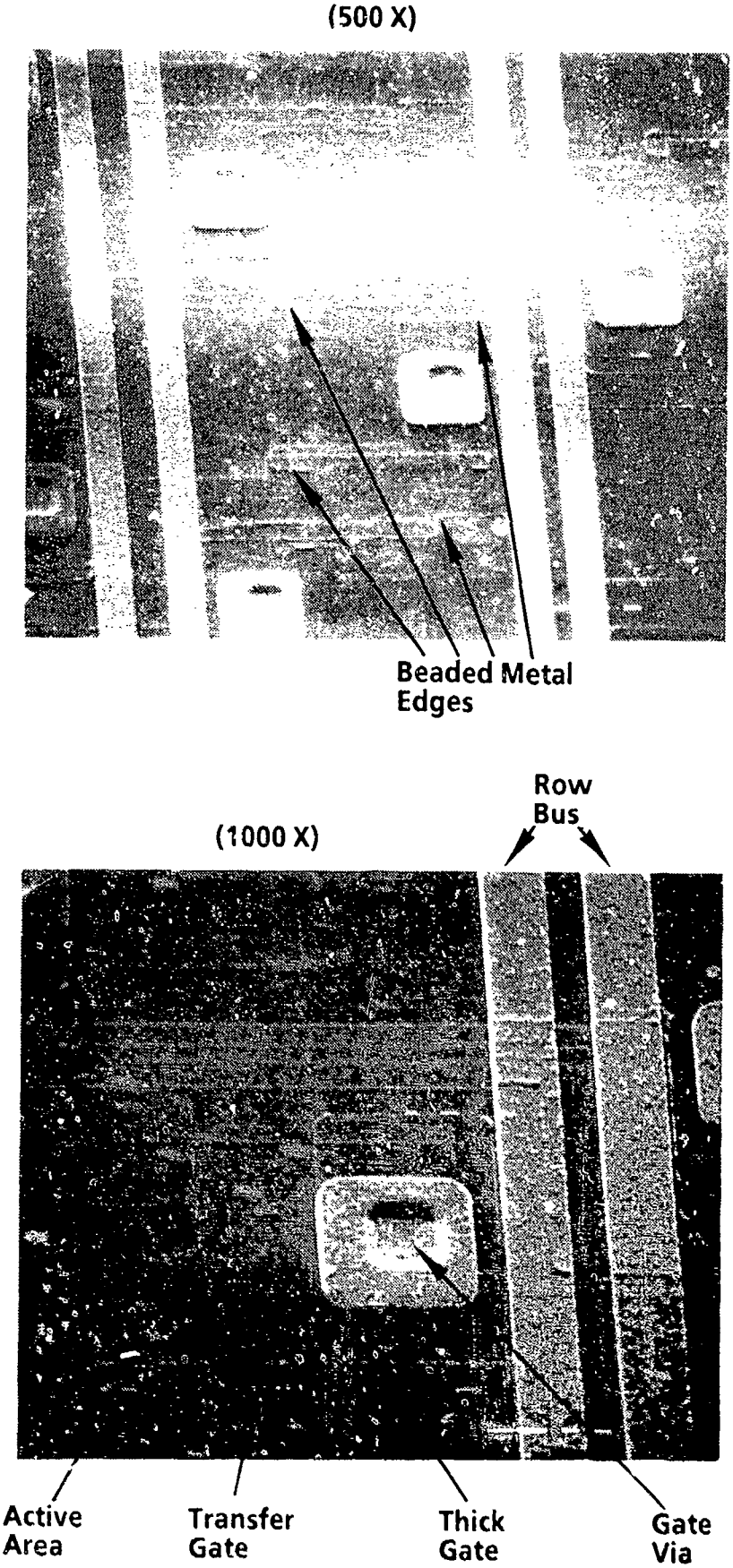


Figure 4-3. SEM micrographs of CIM pixels of IRST array 3A-3 illustrating effects of standard metal liftoff process.

crystal analysis, which localized each of the electrical row defects to individual gate vias. This effect has been shown to arise from small defects in the thin native-oxide layer that comprises the etch-stop for aluminum gate metal, which allow subsequent etchants to penetrate the underlying gate insulator.

Use of the thin-Ni fusible links to isolate shorted pixels and field-plate or transfer-gate segments proved largely unsuccessful on these early array lots because of the high incidence of defects. In general, when two or more electrical defects are present on a given detector row or upper-level gate, competing parallel current paths make it difficult to isolate and open any one fuse unless the resistances associated with the defects differ significantly in magnitude. The fusible-link technique works best when the overall defect count is low, so that most rows (as well as field plate and transfer gate) contain, at most, a single electrical defect.

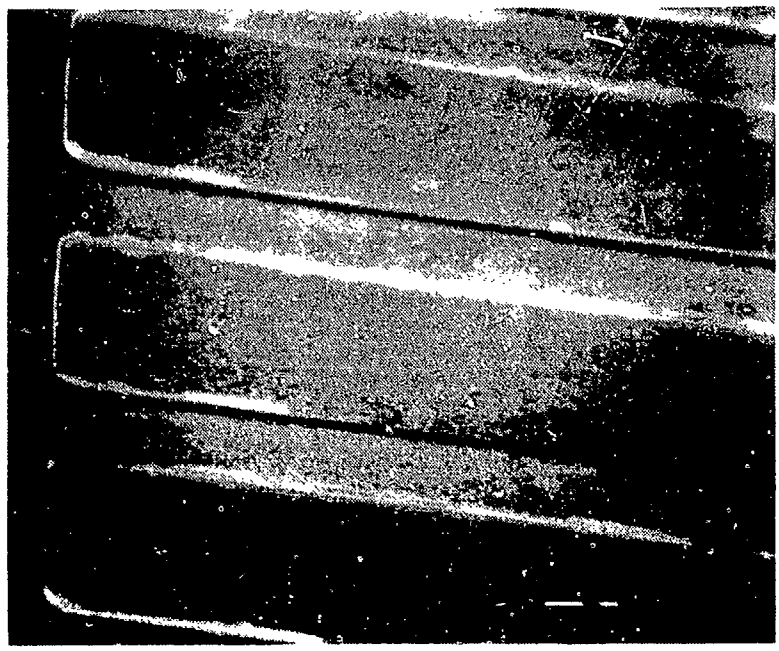
B. PROCESS IMPROVEMENTS AND YIELD ENHANCEMENT

Significant IRST yield enhancement was achieved through several CIM process innovations. The most important of these was the development of an alternative metallization process that replaced lifted aluminum gate electrodes with dry-etched tantalum. This process was first demonstrated on the 128 × 128 large-area CIM and resulted in greatly improved staring-array yields.[21] Figure 4-4 shows a comparison of metal geometries defined by the two techniques. The 120-nm Al pattern defined using a standard photoresist liftoff technique shows pronounced irregularities in edge profile caused by tearing of the Al film during lift. By contrast, the plasma-etch-defined Ta pattern shows a clean edge profile and smooth topography. After subsequent insulator deposition, the effect is compounded, as shown in Figure 4-5: the irregular Al edges cause "beading" of the insulator film (also shown in Figure 4-3), while the coated Ta film shows no irregularities and reflects the clean edge profile of the metal pattern.

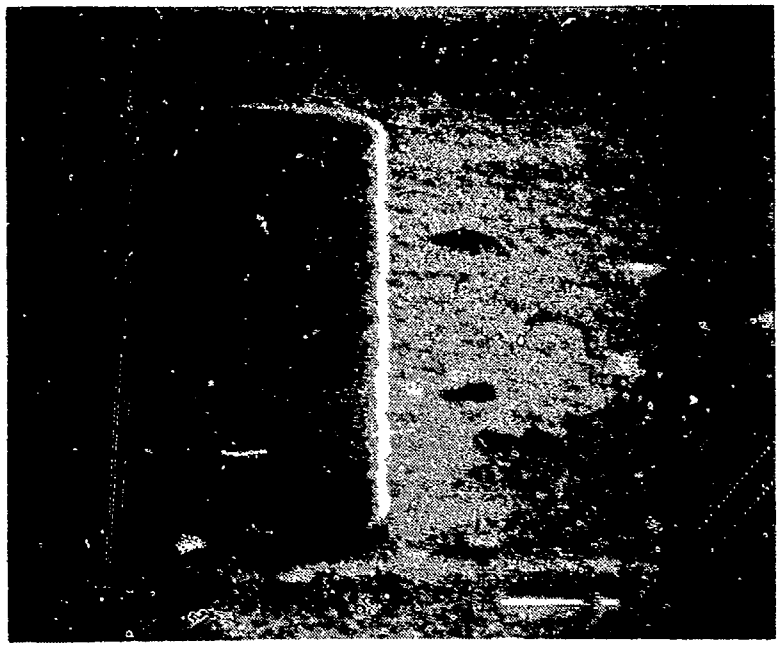
In addition to superior metal edge definition, the dry-etched Ta process offers two other key advantages. First, it provides a positive etch-stop for gate via definition without relying on a native-oxide surface layer, thereby significantly reducing the incidence of via pinholes and resultant gate shorts. Second, as a consequence, it also simplifies the fabrication sequence by permitting partial etching of vias to all gate levels simultaneously. This single process development thus addresses the two major CIM yield-loss mechanisms, i.e., interlevel defects and detector gate shorts.

Other advanced CIM processing features implemented for IRST include:

- Anodic-sulfide surface passivation (ASP), which provides long-term thermal interface stability and facilitates postfabrication diode annealing. Also, the inherent lower fixed-charge density allows upper-level control gates to be operated at reduced bias levels (approximately −1 to −2 V relative to substrate), producing lower insulator stress. ASP

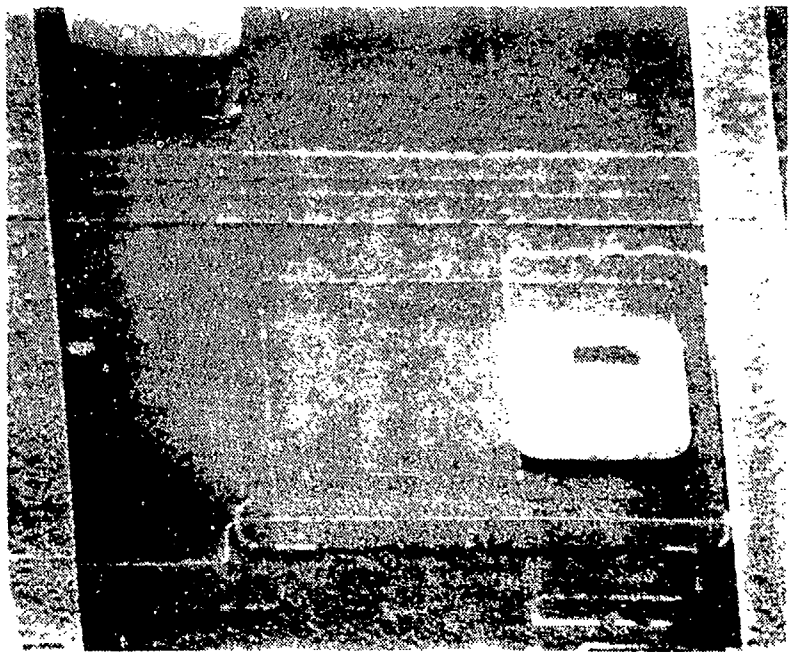


(a)

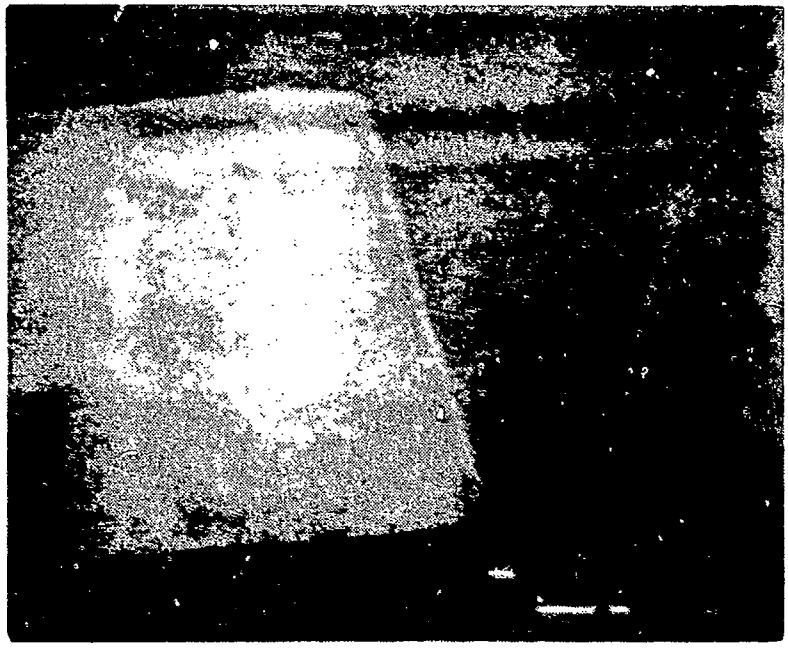


(b)

Figure 4-4. Comparison of edge profiles of liftoff-defined and dry-etched metal electrodes. (a) Lifted 120-nm aluminum electrode; (b) Dry-etched 100-nm tantalum electrode.



(a)



(b)

Figure 4-5. Comparison of surface topology of (a) Completed CIM pixel with lifted aluminum metal patterns, and (b) Dry-etched 100-nm tantalum electrode after subsequent insulator deposition (500 nm ZnS).

is one of several advanced surface passivations developed at Texas Instruments and is now a standard part of the CIM fabrication process.

- MOCVD ZnS for gate insulator, which provides thinner dielectric films of high integrity. This improves gate yields and enhances detector performance through increased MIS well capacity. The same process was subsequently being developed for interlevel insulation as well.
- Direct-step-on-wafer (DSW) projection photolithography, which provides superior pattern definition over the array dimensions of the IRST CIM (approximately 0.80 inch). Early difficulties with the DSW system led to design of an IRST photomask set for use with conventional (proximity printing) photolithography equipment, and this system was used for the first five lots fabricated. With final qualification of the new system, the DSW method was used exclusively from Lot 6 onward.

In addition, toward the end of the contract period, we investigated the use of alternative transparent gate metals (to replace thin Ni). New gate metallizations were developed with demonstrated quantum efficiencies of about 80 percent, comparable to that obtainable with open-window gate structures, but retaining the advantage of a gate-controlled surface potential in the optically active area. However, this process was not implemented for IRST fabrication before the end of the contract period.

The first lot to incorporate all these process advances was IRST 6-E (Experimental), a process-development lot fabricated under internal funding and designed also to investigate the utility of LPE HgCdTe substrates for CIM scanning-array fabrication. For this purpose, MWIR LPE material of 5-μm cutoff wavelength was used. Arrays were fabricated on two large-area (0.8×0.8 in.^{2}) substrates, each of which accommodated the complete IRST photomask pattern consisting of two 480×2 linear arrays, two 480×4 TDI arrays, and two complete blocks of test structures. Figure 4-6 shows a completed sample from this lot, which illustrates the potential advantage of LPE HgCdTe for CIM scanning-array production. A detail of one of the 480×4 CIMs is shown in Figure 4-7.

Room-temperature probe results for lot 6-E are summarized in Table 4-4. All field plates and transfer gates on all eight arrays were nonshorted, and there was a complete absence of interlevel dc shorts. Three linear arrays were defect-free, and four of the remaining five arrays had one defective row each. Overall detector row yield for eight arrays was 94 percent, a vast improvement over results obtained using the previous standard CIM process. CIMs from this lot were sawed and assembled as test vehicles for the IRST test-set electronics, and were evaluated under internal funding.

The last three lots fabricated during the term of the contract were IRST 7, 8, and 9. Lots 7 and 9 experienced incidental processing difficulties unrelated to the newly implemented processes and

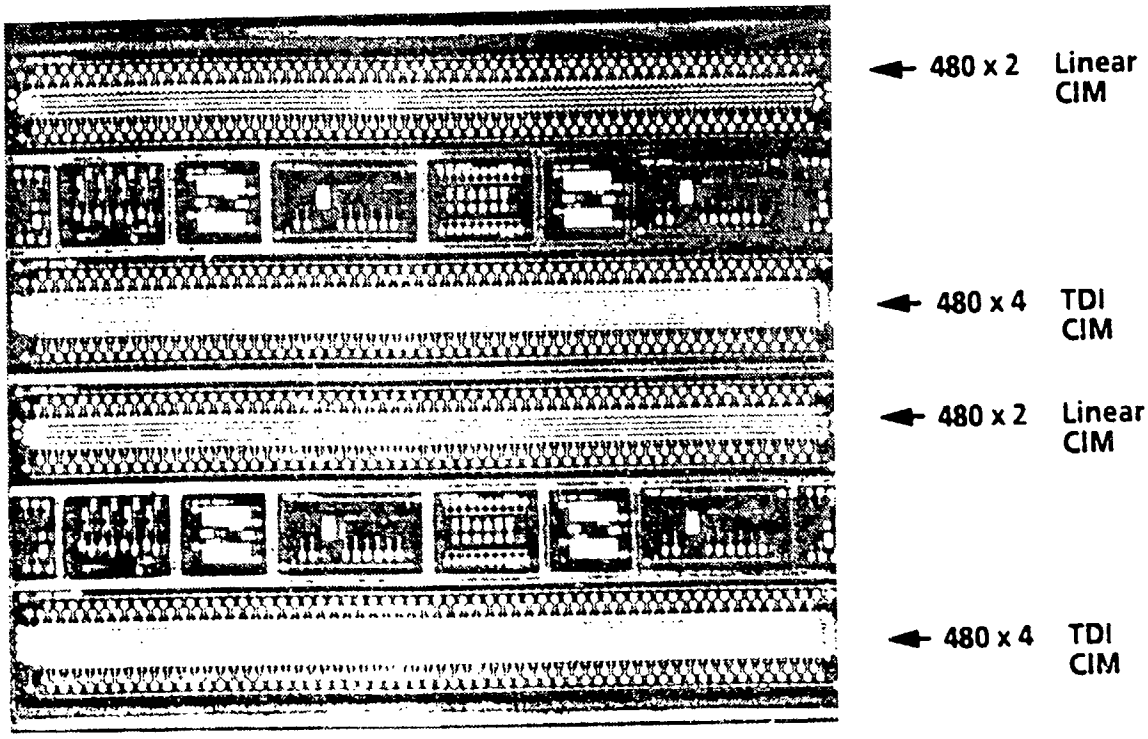


Figure 4-6. Completed sample of IRST development lot 6-E. Each LPE substrate (0.8 × 0.8 in.^{2}) accommodates complete IRST photomask pattern.

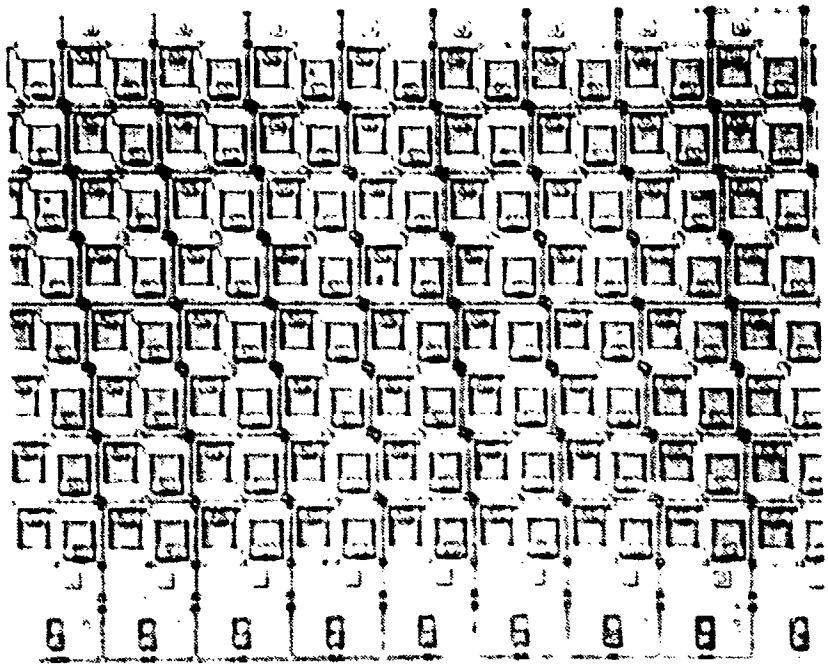


Figure 4-7. Detail of Completed 480 x 4 TID Array From IRST Lot 6-E.

Table 4-4. Probe Yield Summary for IRST Lot 6-E

Array	Type	Substrate Material	Field Plate	Transfer Gate Left	Transfer Gate Right	Row Shorts to Substrate	Row Shorts to FP or TG	Net Row Yield (%)
6E-1-1	Linear	LPE	Good	Good	Good	0 of 8	0	100
6E-1-2	TDI	LPE	Good	Good	Good	2 of 16	0	88
6E-1-3	Linear	LPE	Good	Good	Good	0 of 8	0	100
6E-1-4	TDI	LPE	Good	Good	Good	1 of 16	0	94
6E-2-1	Linear	LPE	Good	Good	Good	0 of 8	0	100
6E-2-2	TDI	LPE	Good	Good	Good	1 of 16	0	94
6E-2-3	Linear	LPE	Good	Good	Good	1 of 8	0	88
6E-2-4	TDI	LPE	Good	Good	Good	1 of 16	0	94

were completed with unacceptable probe yields. Lot 8, however, was completed with excellent yield, and provided the arrays ultimately used for IRST focal-plane evaluation and delivery. This lot is described in Subsection IV.D.

C. MATERIAL SELECTION

The p-type LWIR HgCdTe substrates were selected for IRST lot starts on the basis of prequalified MIS performance data. Initially, intrinsically doped p-type material grown by solid-state recrystallization (SSR) and postannealing was used exclusively. Toward the end of the program, as LWIR p-type LPE substrates became available, these were phased into the last two IRST lots (8 and 9).

Typical MIS characterization data for p-type SSR samples are summarized in Table 4-5. Samples were characterized both at 77 K and 60 K in anticipation of focal-plane operation at reduced temperatures. A minimum MIS dark-storage time of 25 to 30 μs at 60 K was considered adequate for CIM operation at integration times of 4 to 16 μs and temperatures up to 65 K. Substrates were selected for IR cutoff wavelength on the basis of spectral data at 77 K, as also listed in the table. A typical IR response spectrum, determined by MIS C-V modulation measurement is shown in Figure 4-8. This particular sample exhibited dark-storage times of 18 to 35 μs at 77 K and 200 to 650 μs at 60 K. Uniformity of measured IR cutoff across a sample was typically ± 0.1 μm.

LPE substrates were not MIS-characterized before fabrication but were selected on the basis of Hall-effect data; nominal composition; and film thickness, uniformity, and surface morphology. (Typical film thicknesses were about 40 to 80 μm, which would not allow surface rework following MIS characterization.) However, one of the early grown films was characterized; Figure 4-9 shows dark-storage time as a function of substrate temperature for different MIS structures fabricated on the sample. The film was Cu-doped, with an average measured cutoff wavelength of 9.2 μm and a

Table 4-5. Sample of p-Type MIS Characterization Data

Lot No.	Slice ID	Dark-Storage Time (μs) T = 60 K	Cutoff Wavelength (μm) T = 77 K
170	6276-16	50 to 110	10.7
171	1033-42	200 to 750	10.7
174	2307-06	35 to 430	10.2
174	2307-57	50 to 210	10.7
174	2333-56	40 to 280	10.6
174	2333-65	80 to 500	10.5
174	2307-34	200 to 650	10.3
174	2333-42	100 to 3,300	10.3
175	2305-05	40 to 250	11.2
175	2306-32	50 to 250	10.9
175	1030-06	100 to 450	10.4

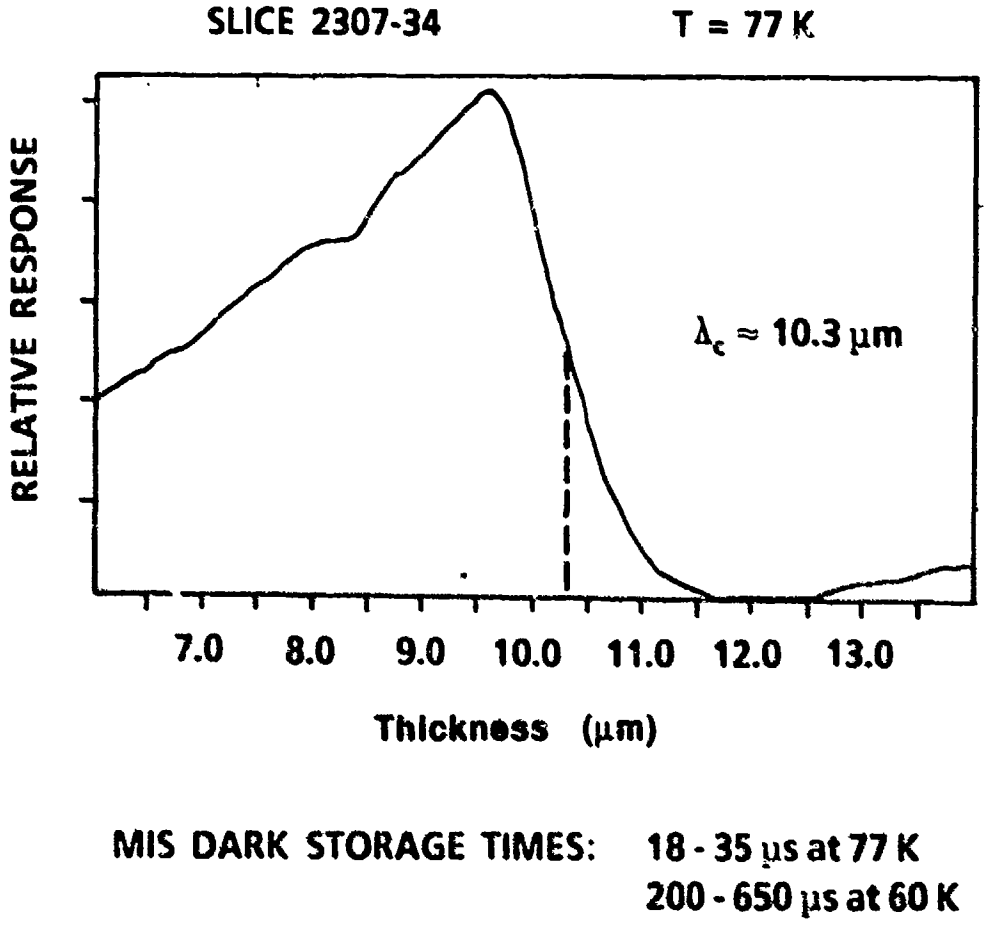


Figure 4-8. Typical IR spectral response for qualified LWIR p-type HgCdTe substrate.

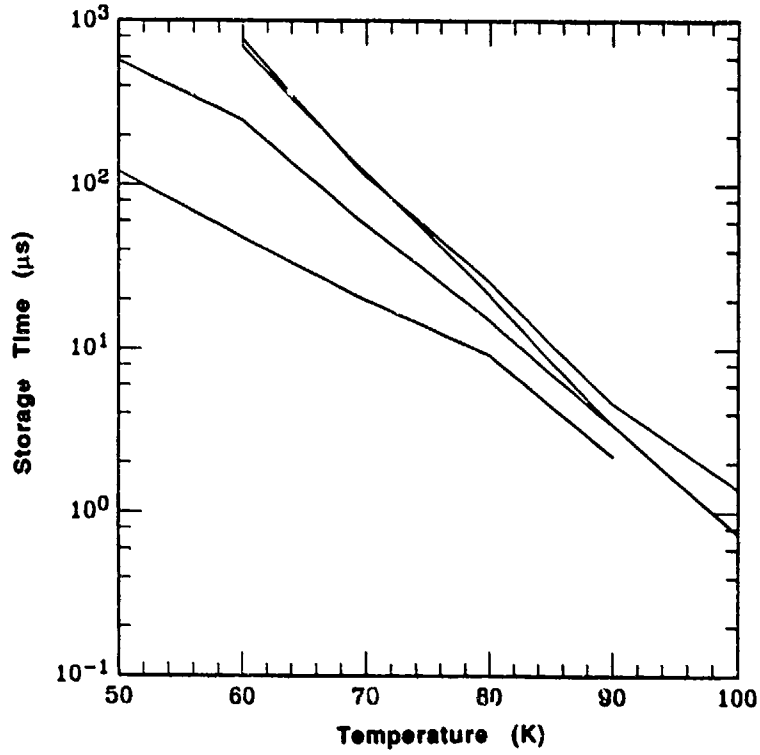


Figure 4-9. Measured variation of dark-storage time with temperature for MIS devices on p-type LPE HgCdTe sample having cutoff wavelength of 9.2 μm.

measured dopant concentration of 6×10^{14} cm^{-3}. Storage times at 77 K were comparable to some of the best SSR LWIR p-type material. Below 60 K, storage times approaching 1 ms were observed. CIMs operated in this temperature range could employ longer integration times with attendant enhancement of detector response.

D. IRST LOT 8B

IRST lot 8, subsequently designated IRST 8B following sample rework early in the fabrication process, was the first LWIR IRST lot to demonstrate superior probe yields. The lot consisted of five SSR and two LPE samples, all containing one 480×4 TDI array. Room-temperature probe data are summarized in Table 4-6. Overall row yield was 95 percent, with one shorted field plate and one defective transfer gate; two interlevel defects were observed on one array. The LPE samples were only large enough to accommodate one array each, and probe yield for these was comparable to that for the SSR samples.

The probe yields shown reflect residual defects that could not be eliminated by fuse isolation. On initial probe, the seven samples of the lot contained a total of three more defects than shown in the table, but these were successfully isolated by opening the appropriate fuse links during probing. The remaining shorts in each case had sufficiently high resistance that the current required to open the corresponding fuse could not safely be generated without risk of damage to the insulator from

Table 4-6. Probe Yield Summary for IRST Lot 8B

Array	Type	Substrate Material	Field Plate	Transfer Gate Left	Transfer Gate Right	Row SLorts to Substrate	Row Shorts to FP or TG	Net Row Yield (%)
037	TDI	SSR	Short to substrate	Good	Good	0 of 16	0	100
044	TDI	SSR	Good	Good	Good	1 of 16	0	94
045	TDI	SSR	Good	Good	Good	0 of 16	0	100
046	TDI	SSR	Good	Good	Good	0 of 16	0	100
048	TDI	SSR	Good	Good	Good	0 of 16	2	88
080	TDI	LPE	Good	Good	Low capacitance	1 of 16	0	94
081	TDI	LPE	Good	Good	Good	0 of 16	0	88*

* Two rows shorted together

Table 4-7. Probe Yield Summary for IRST Lot 10

Array	Type	Substrate Material	Field Plate	Transfer Gate Left	Transfer Gate Right	Row Shorts to Substrate Pre-/Postfuse	Row Shorts to FP or TG Pre/Postfuse	Final Row Yield (%)
394	TDI	SSR	Good	Good	Good	2 of 16/0 of 16	1/0	100
431	Linear	SSR	Good	Good	Good	0 of 8/0 of 8	3/1	88
463	Linear	SSR	Good	Good	Good	0 of 8/0 of 8	3/2	75

the excessive voltage required. On average, about half the process-related defects could be isolated using the fusible links.

Roughly the same success rate for defect isolation was obtained subsequently on probe tests of three high-yielding arrays from IRST lot 10, a development lot fabricated on internal funding. Probe data for these samples before and after attempted fusing is listed in Table 4-7. Of nine electrical defects present at initial probe, six were successfully isolated by fusing (including four of seven interlevel shorts), without visual or electrical damage to the remaining portions of the CIM.

In the case of low-yielding arrays, as discussed previously, the fusible-link technique is generally unsuccessful in isolating more than a small fraction of electrical defects

E. VICIM COMPATIBILITY

The critical added features of the VICIM process flow (Table 4-2) are thinning of the HgCdTe substrate to thicknesses less than 20 μm, permanent mounting of the HgCdTe to a Si processor, and formation of vertical interconnections to the underlying Si. Each of these processes has been developed extensively on other TI focal-plane programs, as described in Subsection IV.A, and present no serious incompatibilities with the optimum CIM process developed on the current program.

One source of initial concern was the observed tendency for thinned p-type HgCdTe to convert irreversibly to n-type (or to apparent poor-quality p-type). This phenomenon has since been shown to result from a combination of mechanical stress in the thinned material and inadequate backside surface passivation. The former effect increases the dislocation density in the substrate (and may cause movement of Hg interstitials), while the latter effect can leave a strongly depleted back surface, providing a source of excess minority carriers with diffusion lengths (in p-type HgCdTe) greater than the substrate thickness; both effects degrade the MIS quality of the HgCdTe surface. As a result of IR&D processing efforts in substrate mounting, thinning, and passivation, these effects have been largely eliminated, and approximately 75 percent of all p-type substrates evaluated show improved MIS character on thinning to 10 μm, as described in Subsection III.E.

Most aspects of the interconnection process are simpler for the VICIM structure than for vertically integrated staring arrays in which a via to Si is required at each pixel site. The VICIM vias occur at the diode output nodes and at row-bus nodes at one end of the CIM array and, thus, may be comparable in linear dimension to a typical pixel geometry. This sizing freedom provides a greater tolerance margin when patterning and etching vias, and permits the use of slightly thicker substrate material (12 to 16 μm) if desired. Via etching occurs just preceding and immediately following the standard CIM process, and the vias are protected by several hundred nanometers of ZnS insulation during standard processing.

The length of the IRST array (0.720 inch active-area length) can impact via uniformity, especially if the substrate thickness is nonuniform across the CIM array, or if the via etch process is inherently nonuniform. The DSW photolithography method helps minimize these effects by ensuring a precise, uniform via pattern over the length of the sample. Improved techniques for mounting and leveling substrates on the processor chip have also contributed to improved thickness uniformity, and the via-formation process is well controlled.

No VICIM lots were fabricated during the contract period. VICIM process development, outside the scope of the program, was conducted as an ongoing effort on internal funding during the second half of the contract period, and the first VICIM IRST lots will be fabricated and tested with IR&D support.

SECTION V
FOCAL-PLANE SIGNAL PROCESSORS

A. OVERVIEW

Two custom silicon IC processors were designed, fabricated, and tested under the 10-μm CIM program by Texas Instruments Focal Plane Electronics (FPE) group. The first, shown in Figure 5-1, is a 480 × 4-element design for time-delay-and-integration (TDI), arranged to interface with an 8:1-multiplexed CIM detector array. The second, shown in Figure 5-2, is a 960 × 1-element design arranged to interface with the 4:1-multiplexed redundant linear CIM detector array. Both processors were combined on a common photomask layout and fabricated using a standard production CMOS process in TI's Semiconductor Group facilities. Both were designed to satisfy the HARPSS system requirements, and, in keeping with long-term FPE goals, the TDI and linear designs also share commonality with ALICAT and ASAM II processors, respectively.

The TDI and linear processors share several common features that helped to ensure first-pass design success and facilitate testing. The most important of these are the digital and analog system-interface blocks. Digital control inputs are TTL-compatible and are arranged on the IC in the same bondpad pattern. Analog inputs and outputs use the same subcircuits and also share the same bondpad pattern. The areas where the two processors differ relate to the detector arrays that are interfaced. The linear processor has dwell accumulation of detector information only; the TDI processor features multiple dwell accumulation in addition to the time-delay-and-integrate function.

B. DESIGN AND LAYOUT

A bar diagram of the redundant linear array processor is shown in Figure 5-3 and a corresponding circuit block diagram in Figure 5-4. Overall size of the silicon chip is 876 × 343 mils. The processor is arranged with analog processing channels on either side of the detector array. Each channel, shown schematically in Figure 5-5, contains one preamplifier, one correlated double sampler (CDS), four pixel accumulators, four threshold correction/dc restores, and four analog multiplexer segments. Voltage and clock inputs are introduced on opposite sides of the processing channels to minimize digital-to-analog crosstalk.

The preamplifier and CDS circuits, shown in Figure 5-6, provide signal amplification and processor noise reduction. In addition, 1/f noise is attenuated from both the preamplifier and the detector. The pixel accumulator, also shown in Figure 5-6, provides signal-to-noise enhancement by summing several samples from the detector in a dwell time. At the pixel accumulators, the signal from the CIM multiplexer is demultiplexed into separate dc-restore blocks. The processor has digital control inputs that select the number of accumulations performed (4, 2, or 1). The dc-restore/threshold-correction circuit, shown in Figure 5-7, is used to remove final offsets from the CIM array and the processor multiplexer.

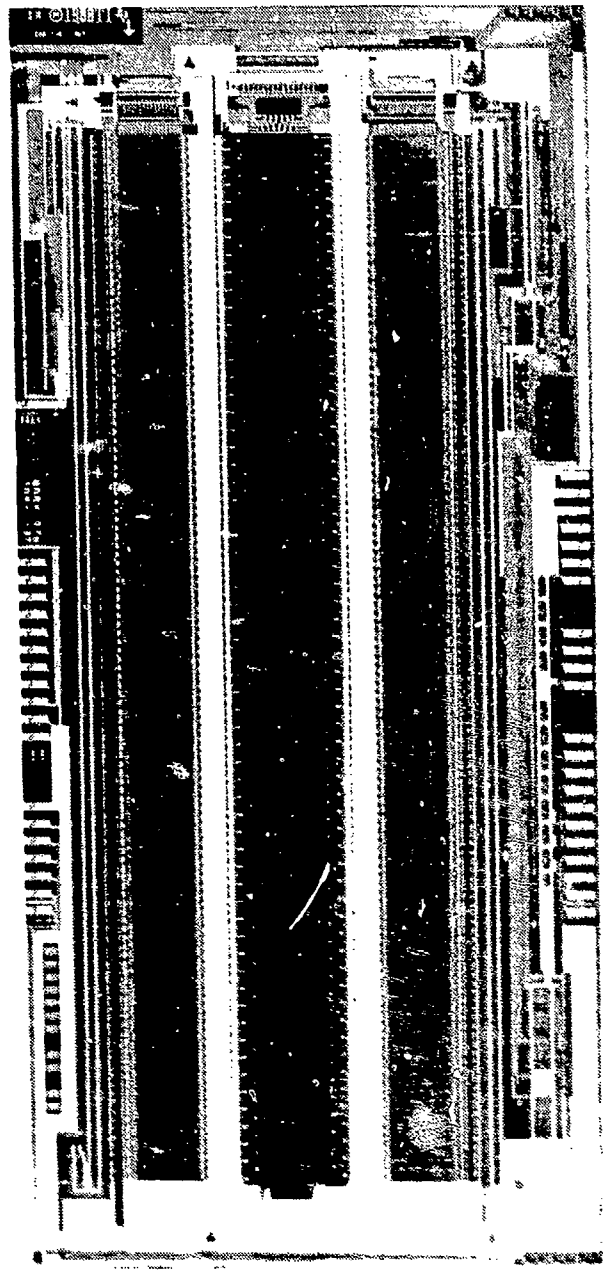


Figure 5-1. Silicon IC processor for the TDI CIM IRST array.

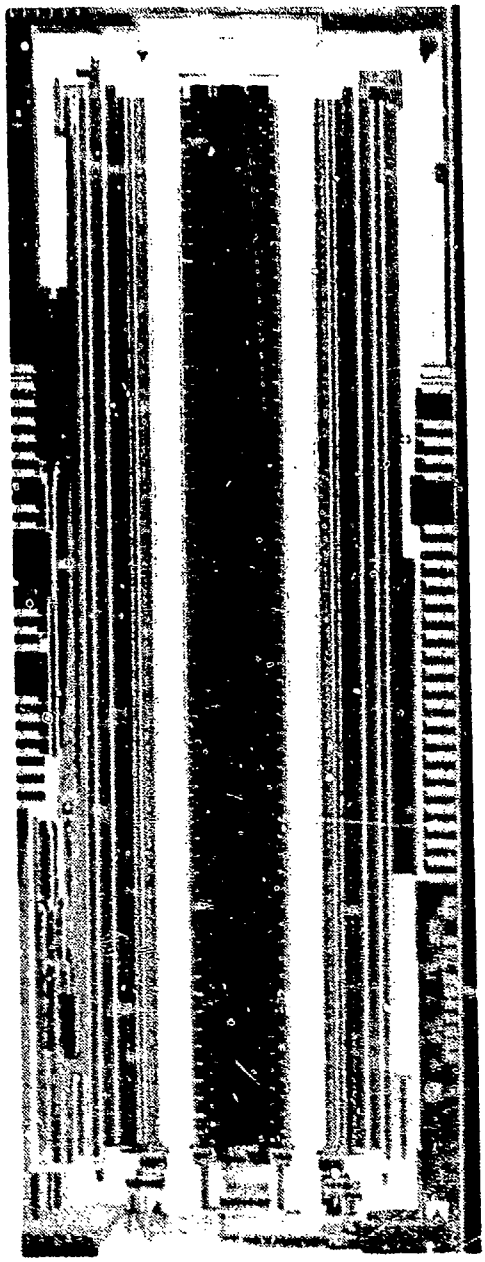


Figure 5-2. Silicon IC processor for the linear CIM IRST array.

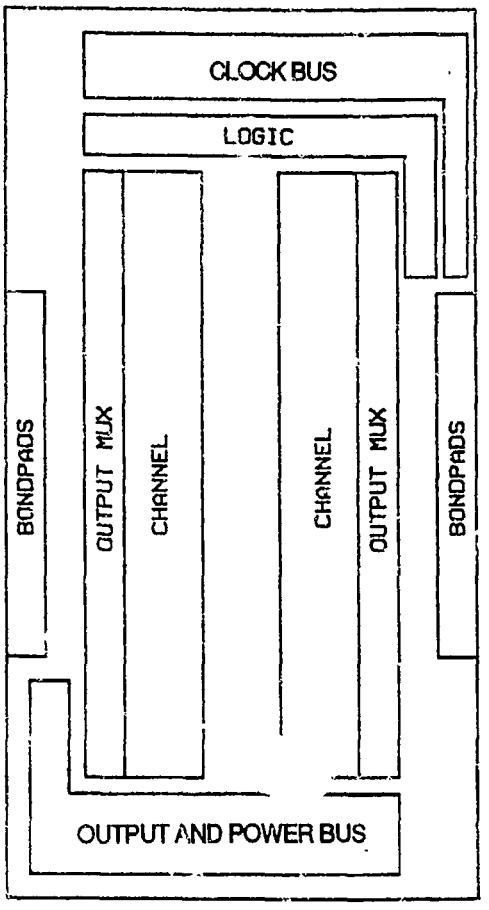


Figure 5-3. Bar diagram of the linear (redundant) array processor.

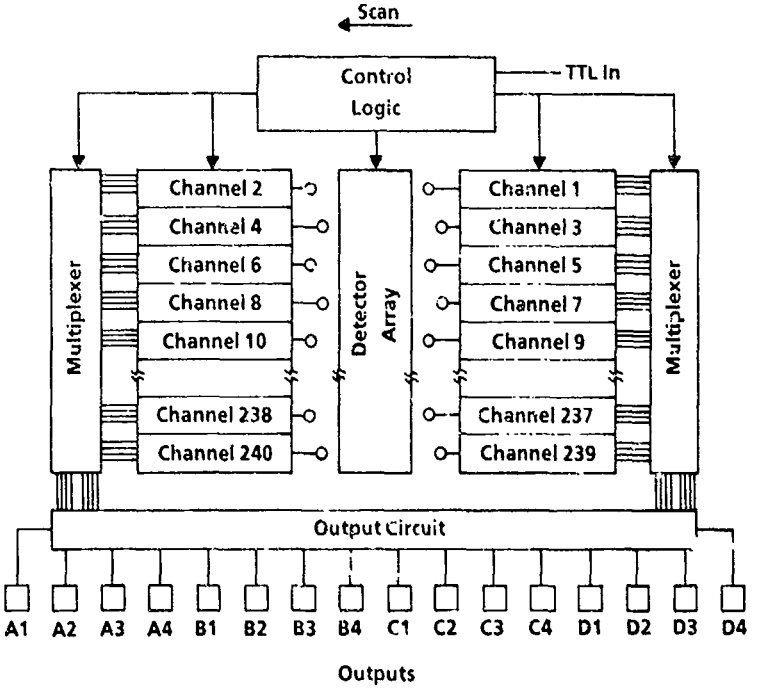


Figure 5-4. Circuit block diagram of the linear array processor.

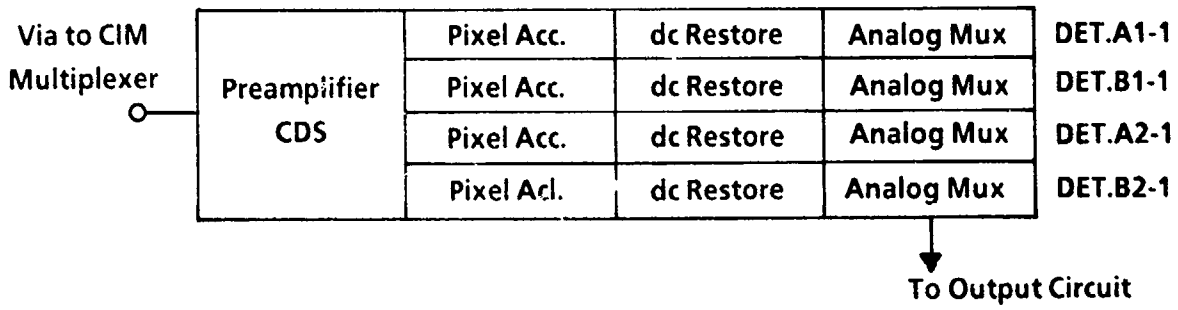


Figure 5-5. One processing channel of the linear array processor.

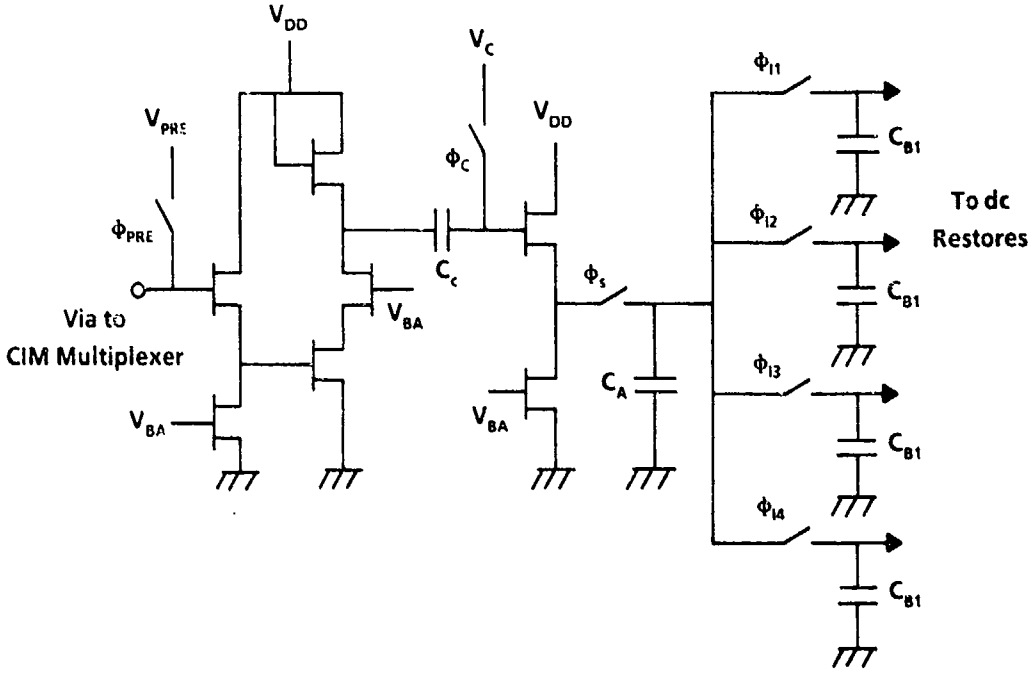


Figure 5-6. Preamplifier, correlated double sampler, and pixel accumulator.

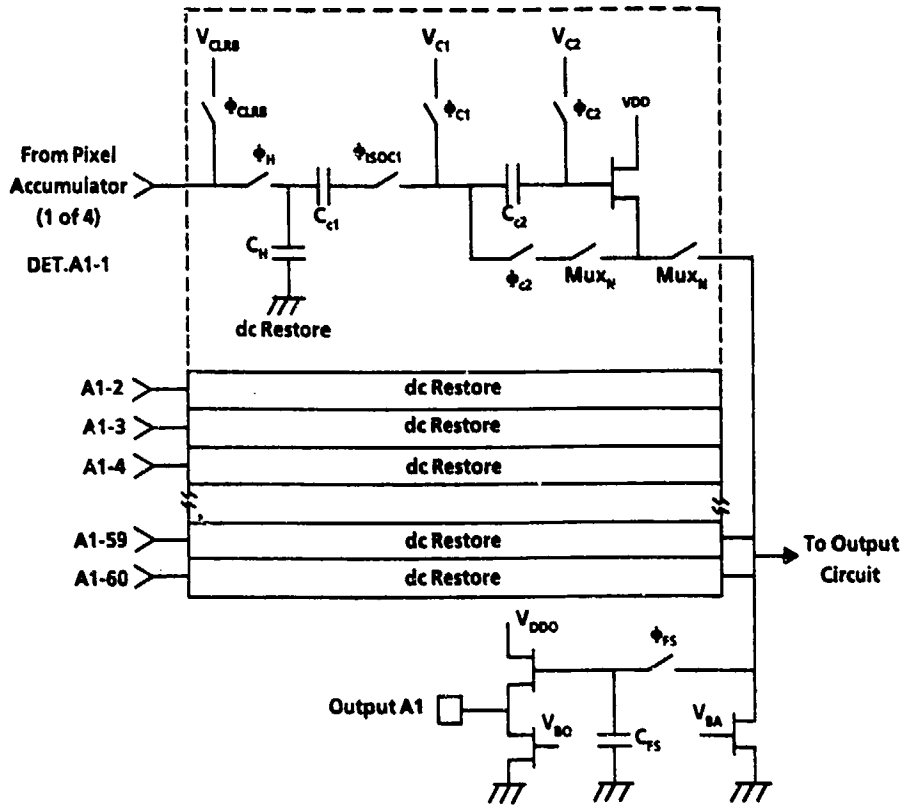


Figure 5-7. DC restore, threshold correction, multiplexer, and output buffer.

An analog-switch common-load multiplexer and output buffer (Figure 5-8) multiplexes the information from every 16th detector onto a separate output line that is sampled and held and buffered for focal-plane output.

The TDI processor, diagrammed in Figures 5-9 and 5-10, has an overall size of 876 × 437 mils, and is also configured with analog processing channels on either side of the detector array. Each channel (Figure 5-11) contains one preamplifier, one CDS, thirty-two TDI accumulators, two threshold correction/dc restores, and two analog multiplexer segments. The other features are identical to those of the linear processor, with the exception of multiple-dwell detector accumulation.

The TDI processor requires the analog storage/summing and digital control logic to perform summing of information from the CIM multiplexer. The eight detectors of the CIM array input to the channel are arranged in two groups of four detectors each. Signals from the detectors of a group are summed synchronously with the optical scan mirror to perform TDI. The control logic, implemented with validated static CMOS logic blocks, keeps track of which TDI storage site is currently summing information on a given pixel.

Both geometric layout and design features were verified by FPE engineers and by Texas Instruments computer-aided design (CAD) tools, such as ADCAP, AST, and Opens and Shorts Checker. Before photomask fabrication, all designs were subjected to a final validation and

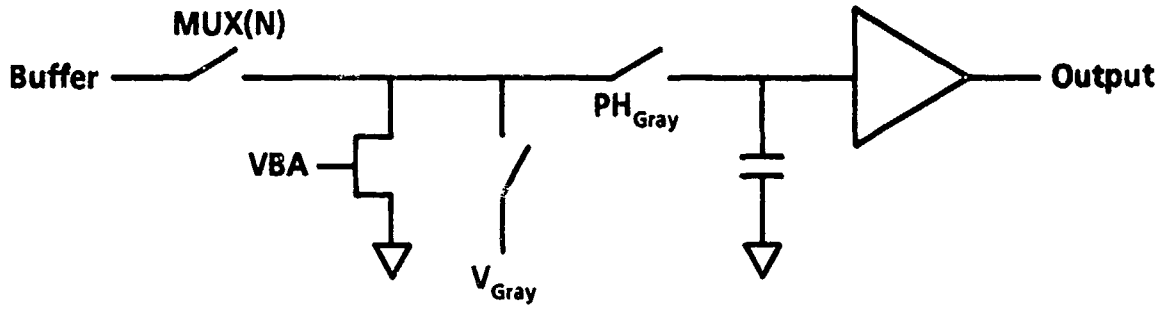


Figure 5-8. Detail of analog-switch common-load multiplexer and output buffer.

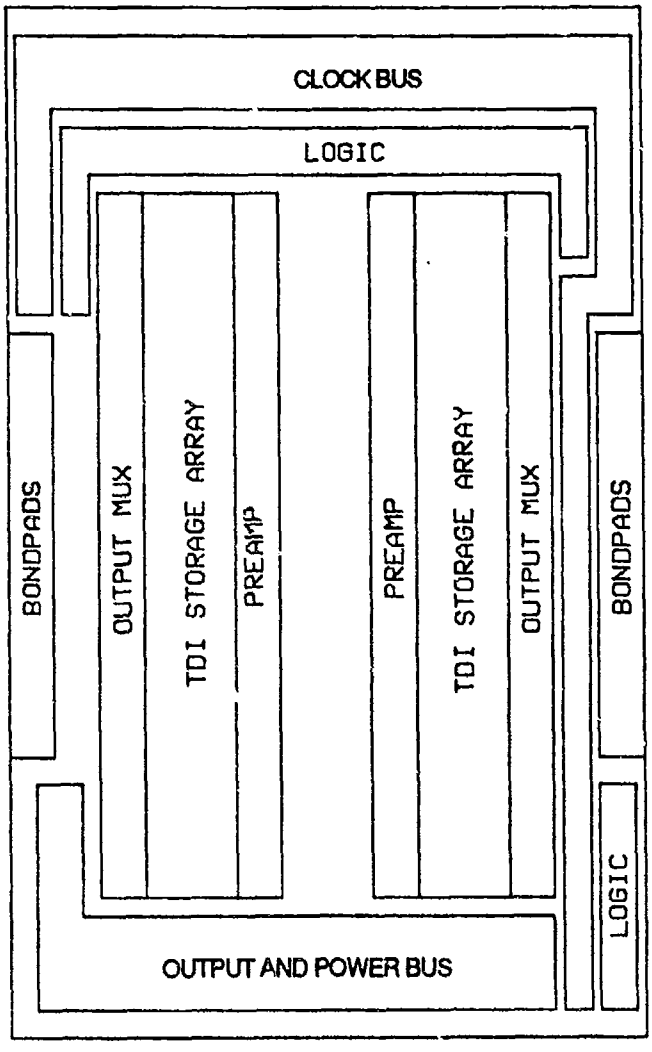
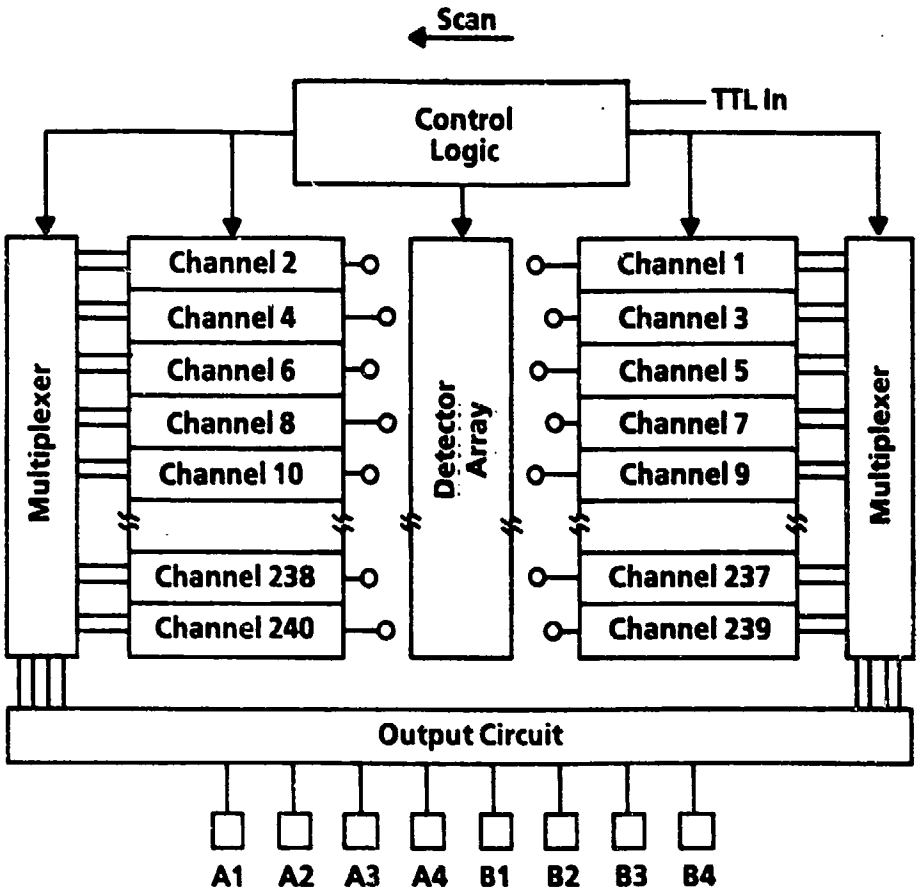


Figure 5-9. Bar diagram of the TDI array processor.



5-10. Circuit block diagram of the TDI array processor.

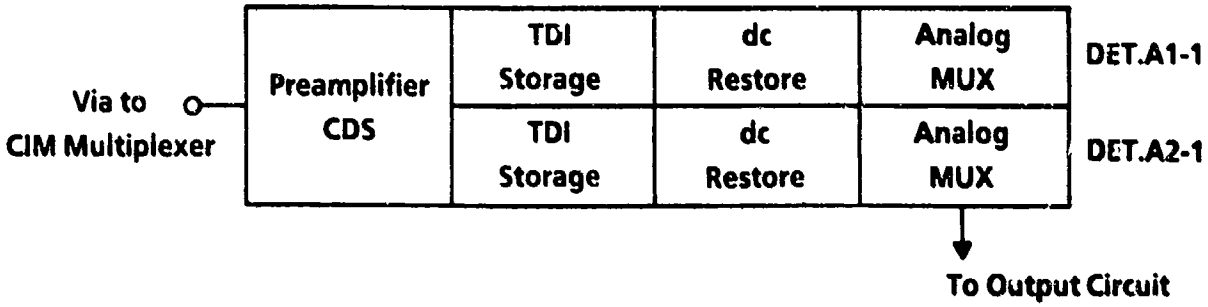


Figure 5-11. One processing channel of the TDI array processor.

verification cycle that included critical design reviews among FPE design engineers, DSEG system engineers, and IDL engineers and program management.

Photomask pattern layout was arranged to provide eight TDIs and eight linear processors on a 4-inch-diameter silicon wafer, as shown in Figure 5-12. The wafer also contains four plugs, one at each of the vacant corners. Each plug comprises two each 128-, 64-, and 32-channel addressers as well as processor and process test structures. A typical fabrication lot would consist of 22 wafers, containing a total of 176 processors of each type. Based on typical defect densities for these chip sizes, a projected fabrication yield of 15% was expected, or approximately 26 good chips of each type per lot. To facilitate FPE testing and yield evaluation, one test input and two digital test output bondpads were included on each processor.

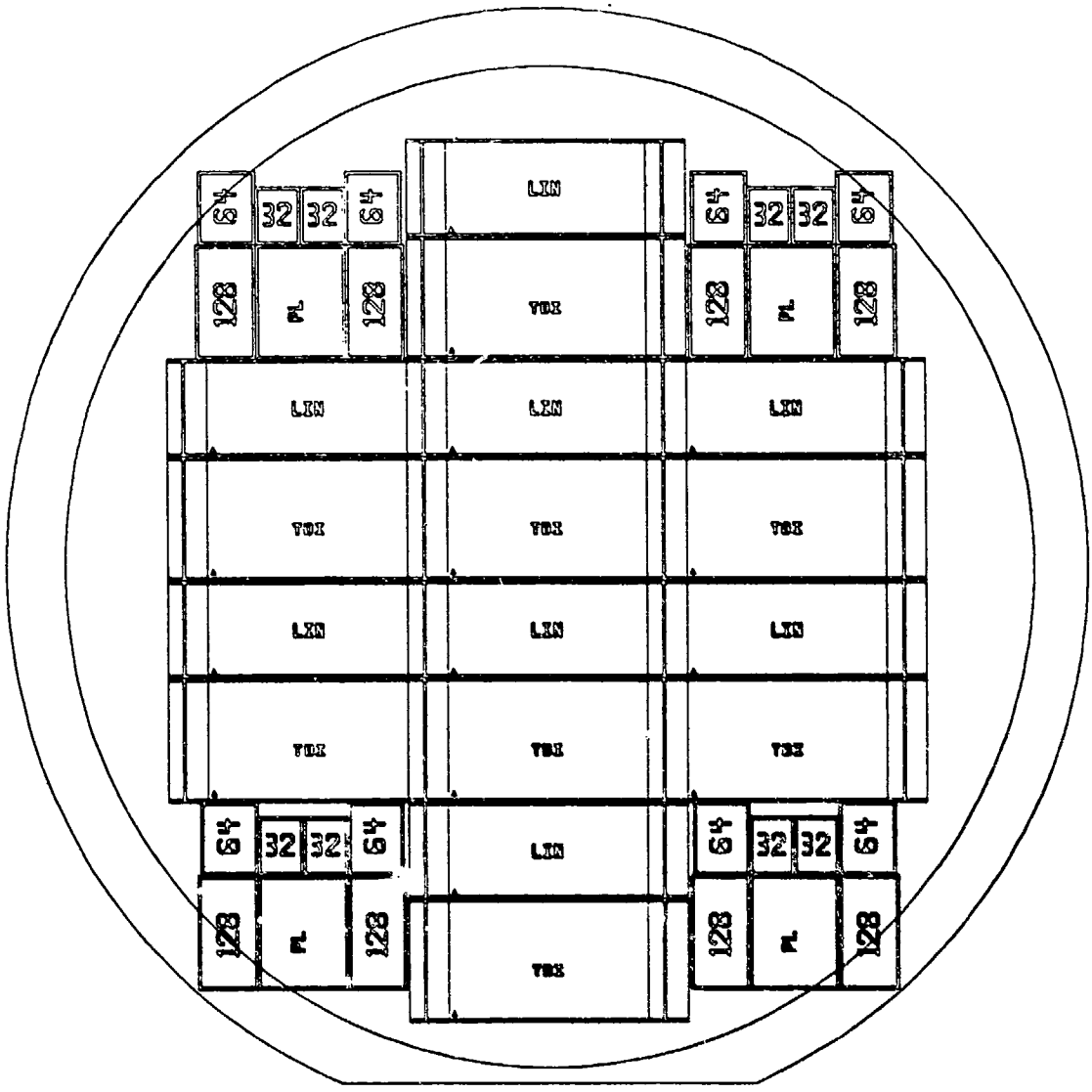


Figure 5-12. Pattern layout of TDI and linear processors on a 4-inch-diameter silicon wafer (shown enlarged).

C. PERFORMANCE EVALUATION

The first two fabrication lots were misprocessed, but five wafers from the second lot were found to have nonzero yield; samples of both processors were identified from these wafers for performance evaluation by FPE engineers. No indication was found of design or layout errors on either device type, eliminating the need for a costly design revision phase.

The dc and ac characterization of both processors demonstrated that all internal logic was connected and operating correctly. Table 5-1 shows the required and measured values for gain, power dissipation, data rate, and input-referred noise for both processors at 77 K. (Measured values are for the four-accumulation mode; for the other modes, gain, power, and noise will change.) All measured parameters were found to meet or exceed their design requirements, most significantly for power dissipation and noise.

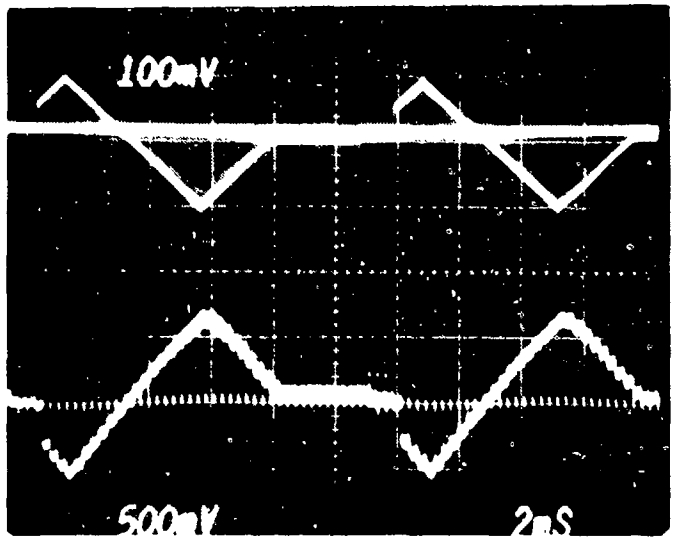
Figure 5-13(a) shows an input analog waveform and one of 16 outputs from the linear processor, measured at room temperature. Each line on the output is composed of 60 bits of video and 4 gray bits. (The gray bits are in the middle of the output waveform.) Figure 5-13(b) shows the input and one of eight outputs from the TDI processor, also at room temperature. Because of the four TDI stages, the output requires four exponential steps to respond to the input change. Because the TDI is four deep, each step is composed of four lines. Each line has 60 bits of video and 4 gray bits, as for the linear processor.

D. FABRICATION YIELD AND DEVICE INVENTORY

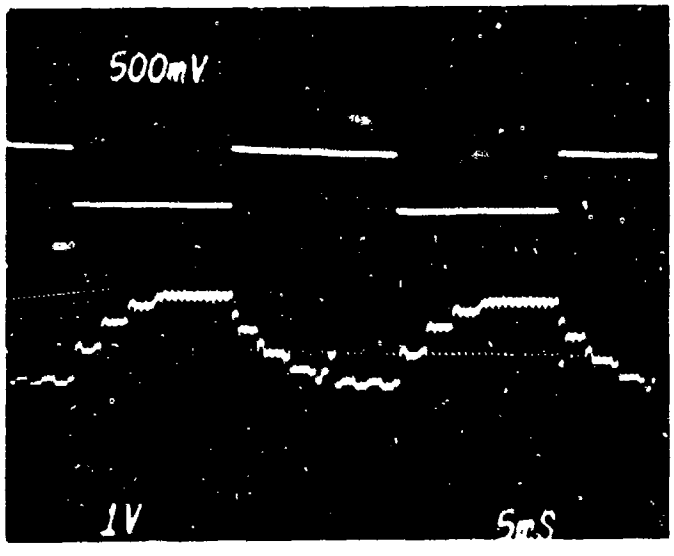
A total of five processor lots were fabricated in TI's Semiconductor Group facilities. Of these, the first, second, and fourth lots were misprocessed and yielded only the five wafers described previously from the second lot. The yield of functional chips from these wafers was 20% for the TDI and 10% for the linear processor. Average yield was only slightly lower than expected and was consistent with the processing difficulties encountered with this lot.

Table 5-1. IRST Silicon Processor Parameters

Parameter	TDI		Linear	
	Actual	Required	Actual	Required
Gain	6	3	7.5	5
Power (mW)	320	< 400	350	< 400
Data rate (MHz)	1.25	1.25	3.0	3.0
Noise (input-referred) (μV)	—	< 20	18	< 20
Detector elements	480 × 4	480 × 4	480 × 2	480 × 2
Outputs	8	8	16	16
Accumulations	4, 2, 1	4	4, 2, 0	4
Output MPX	64:1	60:1	64:1	60:1
Gray levels	4	4	4	4



(a)



(b)

Figure 5-13. **Input and output waveforms (at room temperature) for the IRST silicon processors: (a) linear processor, (b) TDI processor. The TDI response to a square-wave input shows the characteristic exponential rise and fall.**

The third and fifth lots yielded significant numbers of functional chips of both types. Yield results for these lots are summarized in Table 5-2. The 34 wafers tested provided a total of 67 TDI and 50 linear processors that were 100% functional (i.e., met all room-temperature dc/ac requirements), plus an additional 17 marginal chips (14 TDI, 3 linear) suitable for process-development studies. The functional yield on the fifth lot--36 percent--was greater than twice the projected value, and marginal chips from this lot were not dispositioned. Together, these lots provide a sufficient processor inventory for all projected VICIM FPA development, both TDI and linear.

Table 5-2. IRST Silicon Processor Yields

Lot	Type	No. Tested	DC Yield (percent)	DC/AC Yield (percent)	No. Good	No. Marginal
19711	TDI	136	45	15	20	14
	Linear	136	69	0	0	3
21793	TDI	136	42	35	47	
	Linear	136	62	37	50	

Total processor inventory: 67 TDI, 50 linear

SECTION VI
FPA TEST SYSTEM

A. GENERAL ARRANGEMENT

The IRST FPA electronic test set was designed to be a compact, low-noise, user-oriented, mechanically variable and expandable benchtop system. A key ingredient in the system design was the incorporation of user-variable timing software, intended to provide maximum versatility in CIM operation and troubleshooting. With this feature, any combination of timing and power installations to the CIM FPA would be possible, and any linear or area CIM array could be operated with suitable modification of the system software.

The IRST test set as originally configured for the bondable 480 × 1 CIM/HDP focal plane is illustrated schematically in Figure 6-1. The system consists of (1) a Hewlett-Packard 9000-series computer; (2) a Pulse Instruments 5800A timing pattern generator; (3) a power supply and driver rack, containing 32 PI 451 MOS drivers and 15 compact HP power supplies; (4) a TI-modified Kadel cryogenic dewar module; and (5) assorted printers, oscilloscopes, and display monitors.

The master clock timing to the CIM/HDP focal plane was limited to the range dc to 50 MHz. This is the only significant range limitation on the system operating parameters. Noise performance goals require that excess system noise at the CIM output be dominated by the input reference noise (9 to 12 μV) of the silicon HDP processor; further, the HDP is limited by an operating bandwidth in the range of 1.5 to 2.0 MHz. These constraints place practical limits on the actual clocking rates used, even though the system and software design permit broader limits of operation.

The FPA test set was subsequently modified following acquisition of a Pulse Instruments 4000-series low-noise FPA integrated benchtop test system in the third quarter of 1989. Incorporation of the new electronics required substantial modifications to the system software and hardware, but promised to provide significant improvements in excess system noise and power-supply drift. The new system was installed and operational before arrays from IRST Lot 8B were tested.

B. LIQUID NITROGEN DEWAR MODULE

A modified Kadel 9-inch-diameter liquid nitrogen (LN_2) test dewar was employed for low-noise performance and maximum flexibility. The design was adapted from one constructed for the large-area CIM test program under NRL Contract N00014-86-C-2193.

The dewar is illustrated in cross section in Figure 6-2. The previous design was modified to extend the dewar window and cold-shield aperture approximately 1 inch farther from the focal plane. This was necessary both to obtain the required background flux densities (uniformly across the detector array) and to optimize the optical design for use of 1-inch-diameter layered-dielectric bandpass filters. The filter is positioned 0.06 inch from the CIM package; this step is critical since

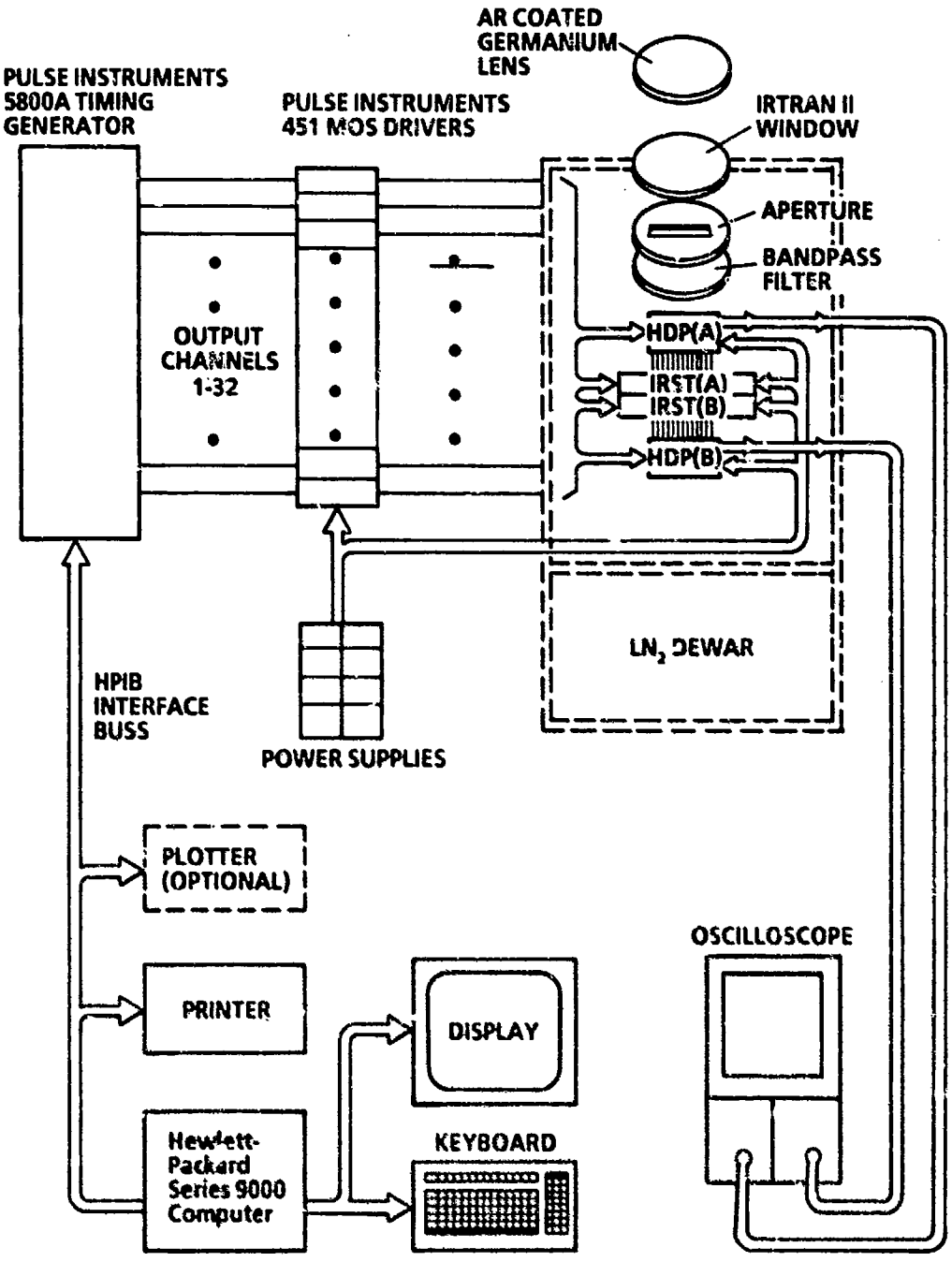


Figure 6-1. Block diagram of IRST FPA test set, original configuration.

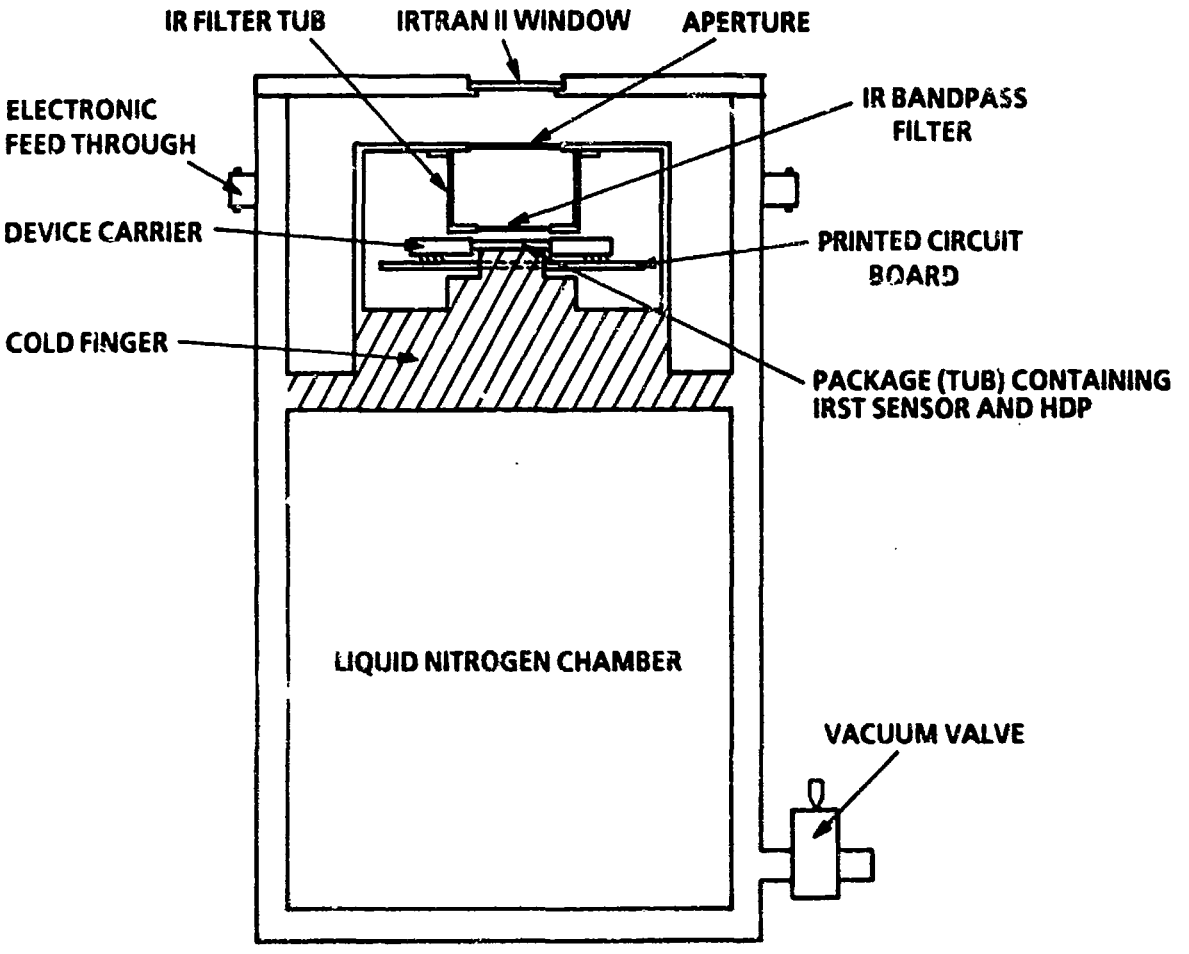


Figure 6-2. Cross section of 9-inch-diameter CIM LN_2 Dewar assembly, shown in assembly position (upside down).

any stray radiation on the focal plane would degrade image quality. Precise filter placement was accomplished by fabricating a tub-shaped (inverted "top-hat") holder, as shown in Figure 6-3, and securing it to the backside of the cold shield. This arrangement is shown in detailed cross section in Figure 6-4, along with the external system optics, discussed in a subsequent section.

External connection to the CIM focal plane is accomplished using electrical feedthroughs, coaxial cabling, printed circuit board (Figure 6-5), and a TRW cinch connector to the CIM package. To minimize induced (excess) noise, low-temperature coaxial cable was used for all dewar wiring wherever possible. The outside perimeter of the dewar has a total of 98 connections available for timing, power supply, and output signal lines to and from the focal plane; 38 of these are required for normal operation of both sides of the linear, bondable IRST array.

C. FPA PACKAGE

The package used for the 10-μm IRST/HDP focal-plane array is a standard 96-pin Textool tub in a plastic carrier. Detector and processor mounting and interconnection are accomplished using

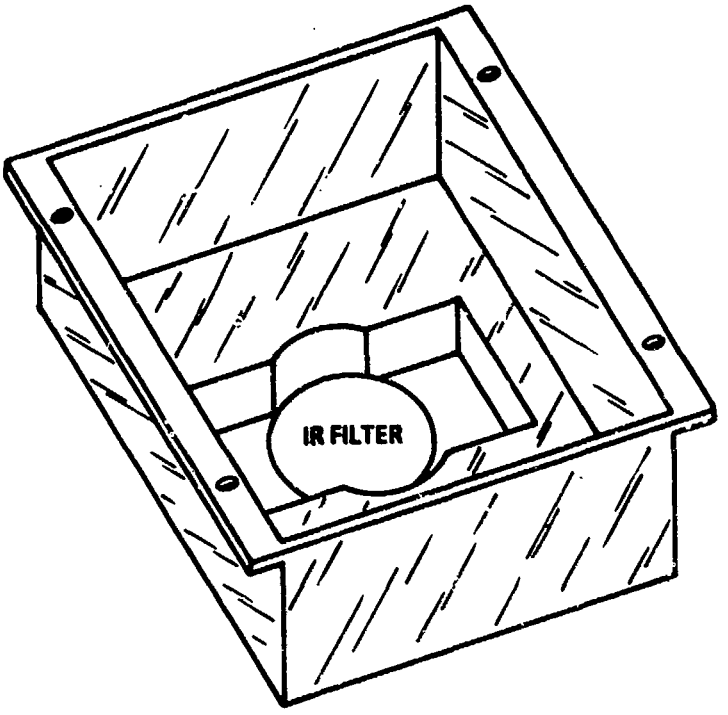


Figure 6-3. "Inverted top hat" cold-shield fixture for mounting layered-dielectric IR filter.

a custom-designed ceramic carrier assembly, illustrated in Figures 6-6, 6-7, and 6-8. The composite carrier design superimposed on the 96-pin package layout is shown in Figure 6-9.

Focal planes assembled for demonstration used prequalified HDPs to multiplex signal outputs to the external interfaces. The HDP is a silicon integrated circuit, illustrated schematically in Figure 6-10, that provides detector reset operation, impedance transformation, buffer amplification, correlated double sampling, and output multiplexing. Test results obtained using prequalified HDPs in the IRST dewar module are reviewed in Subsection VI.E.

Since the linear IRST CIM is actually two independent sensor arrays on one device, and since these are symmetric when rotated by 180 degrees, "right-hand" or "left-hand" HDP designs may be used for both arrays. The package, ceramic design, and electrical connections are simply rotated by 180 degrees from one side of the tub to the other. With this configuration, both detectors can be operated in conjunction or separately using appropriate software options.

D. OPTICAL DESIGN

The optical design developed for the 10-μm IRST FPA is illustrated in Figure 6-11. The design allows both detector arrays (shown as upper and lower IRST) to be illuminated with the same set of optics, without need to translate either the FPA carrier or the optical image of the far-field scene.

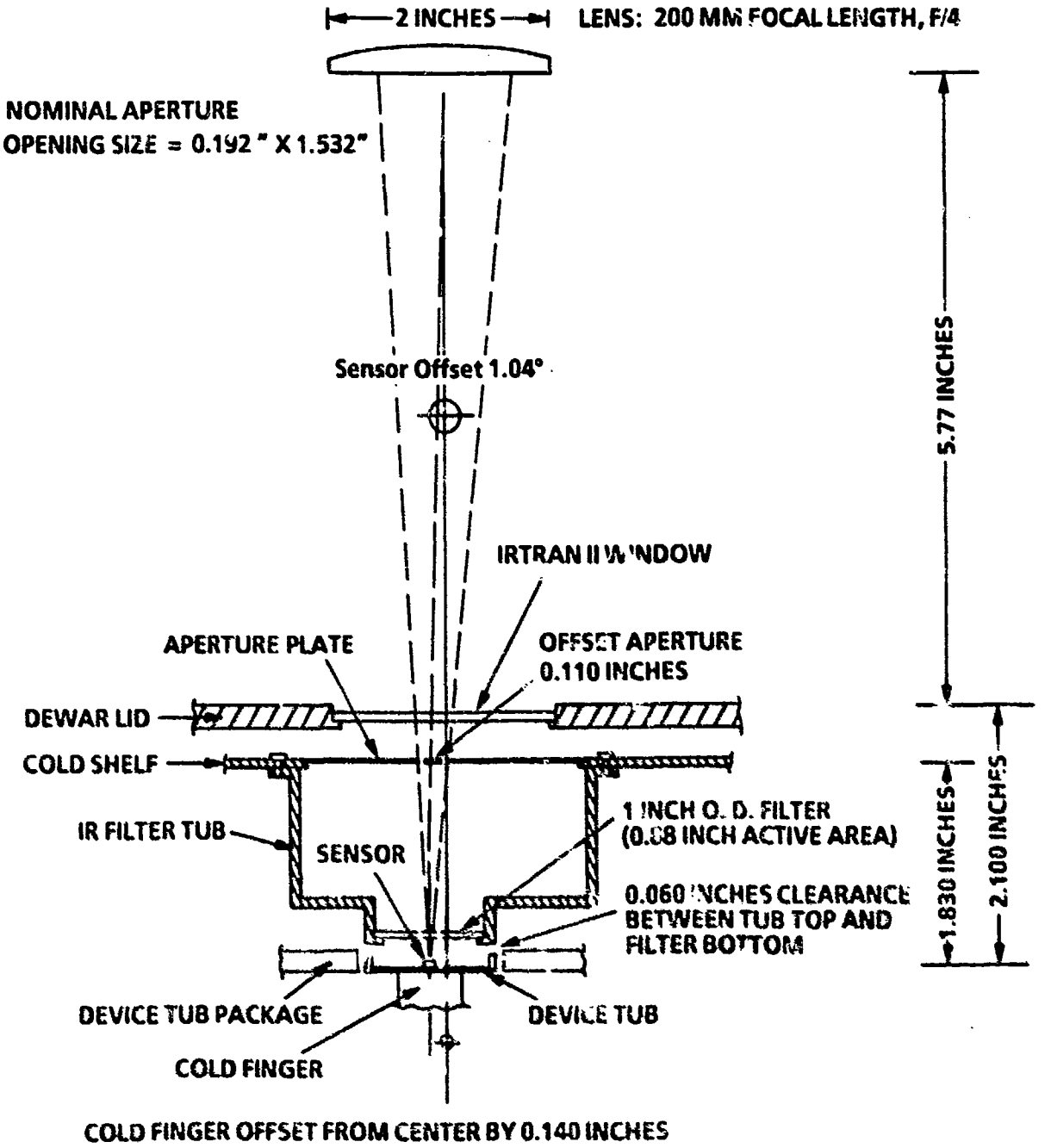


Figure 6-4. Cross section of IRST cold-shield configuration and system optics.

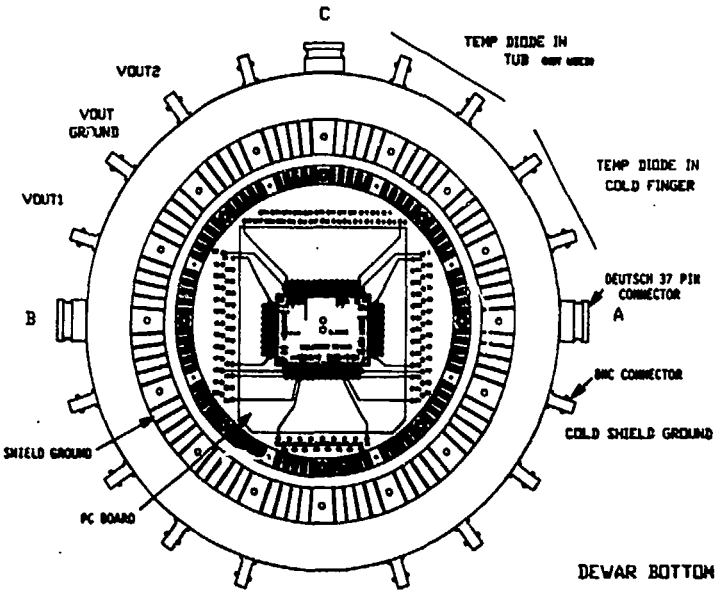


Figure 6-5. Dewar cross section in plan view, showing printed circuit board and external electrical connectors.

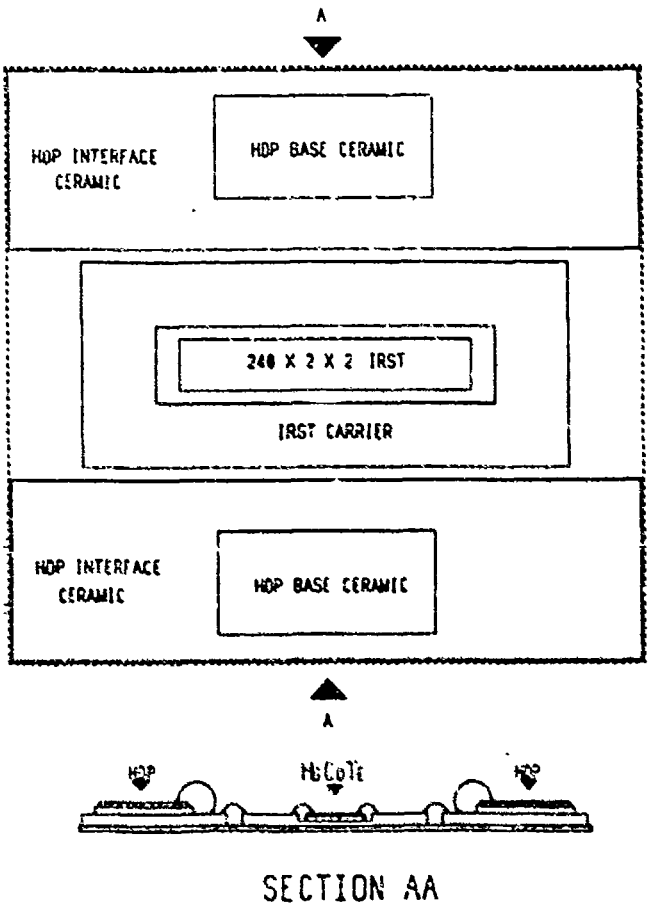


Figure 6-6. Schematic diagram and cross-section of linear, boodable IRST ceramic carrier design.

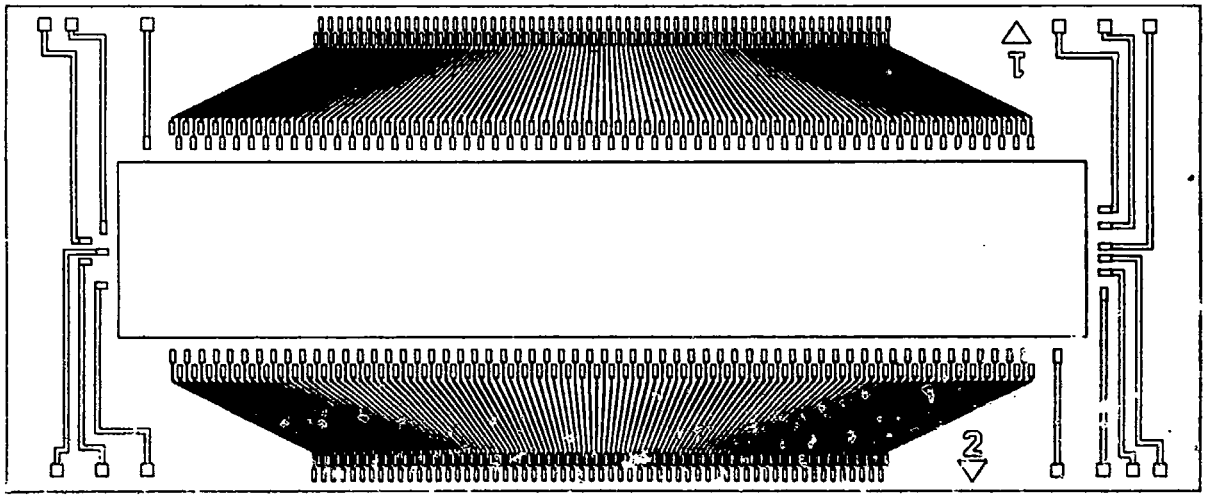


Figure 6-7. Linear IRST array carrier design.

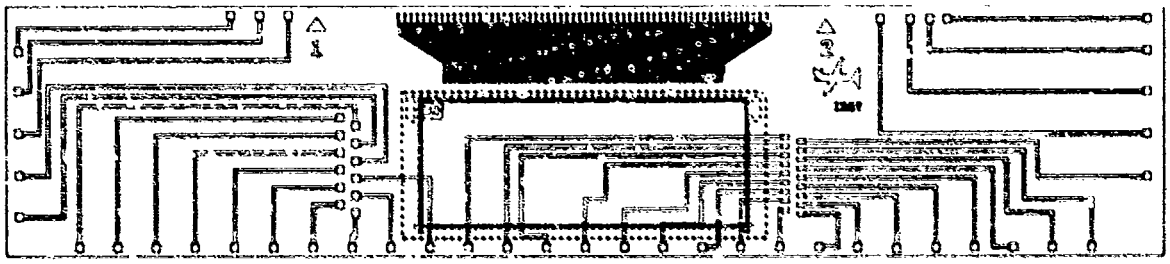


Figure 6-8. Silicon HDP interface carrier design. The dashed rectangle is the outline of the thin base ceramic that isolates the silicon processor from the metal leads on the interface carrier.

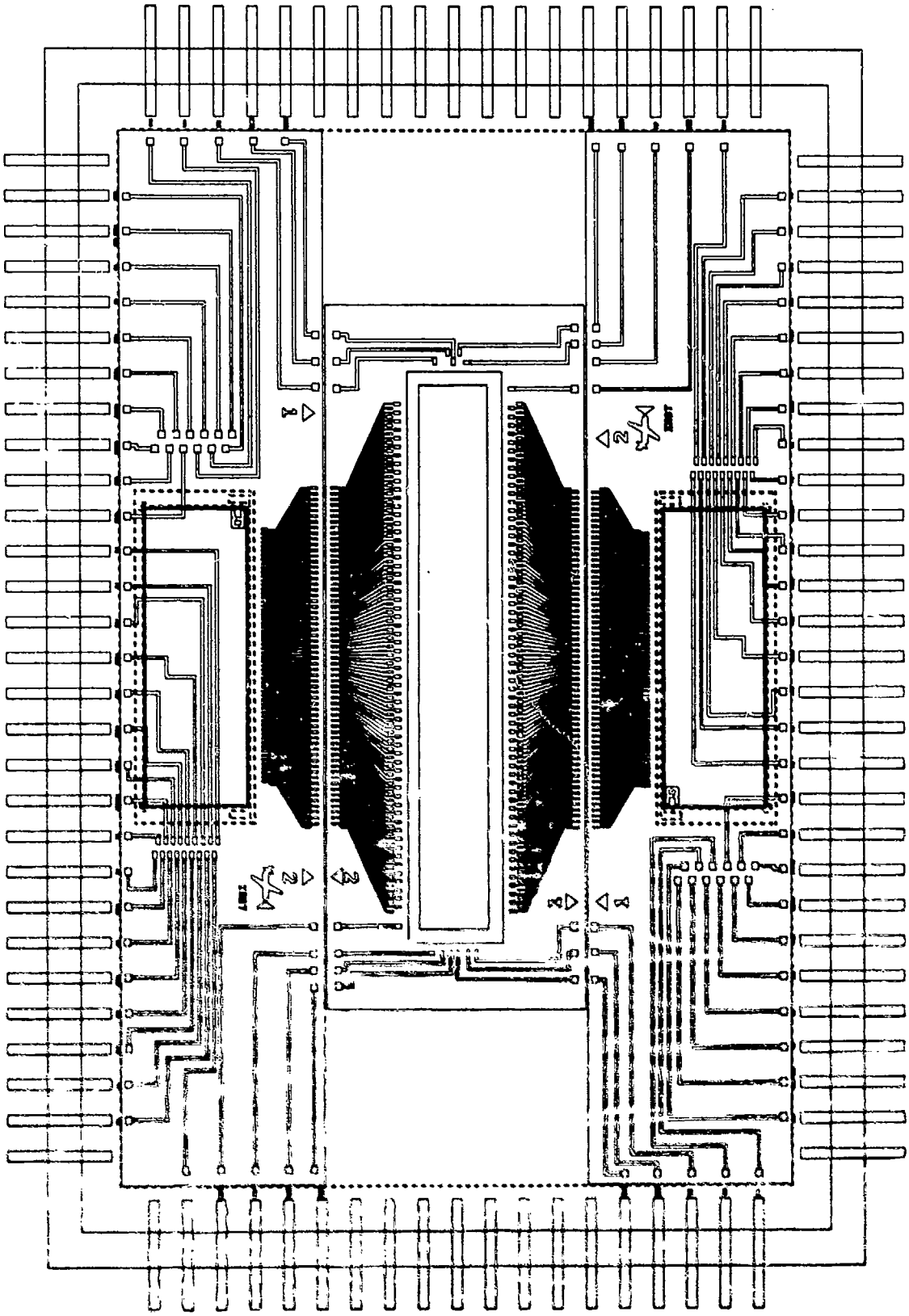


Figure 6-9. IRST composite carrier design in standard 96-pin package layout.

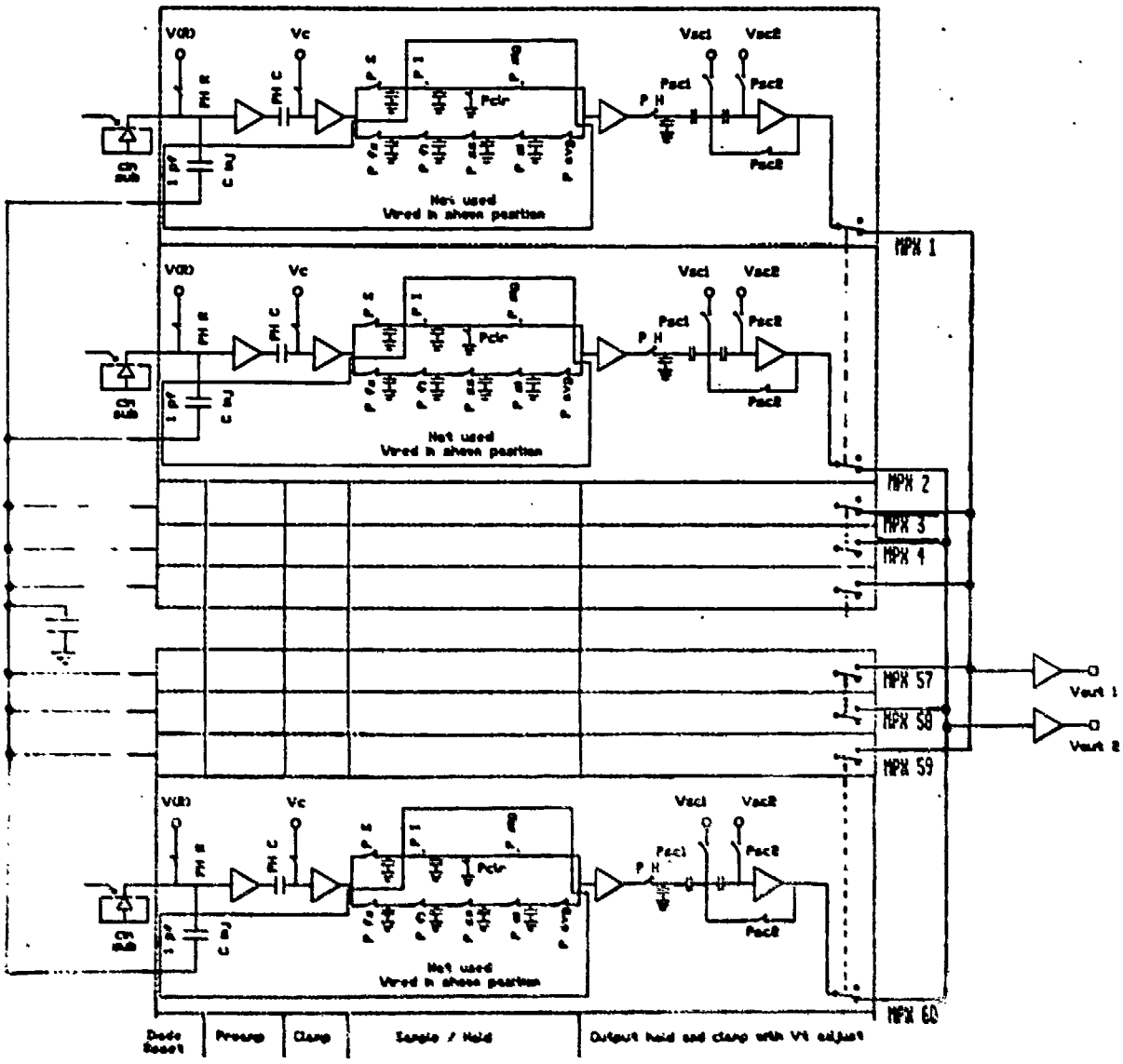


Figure 6-10. Silicon high-density processor (HDP) circuit design.

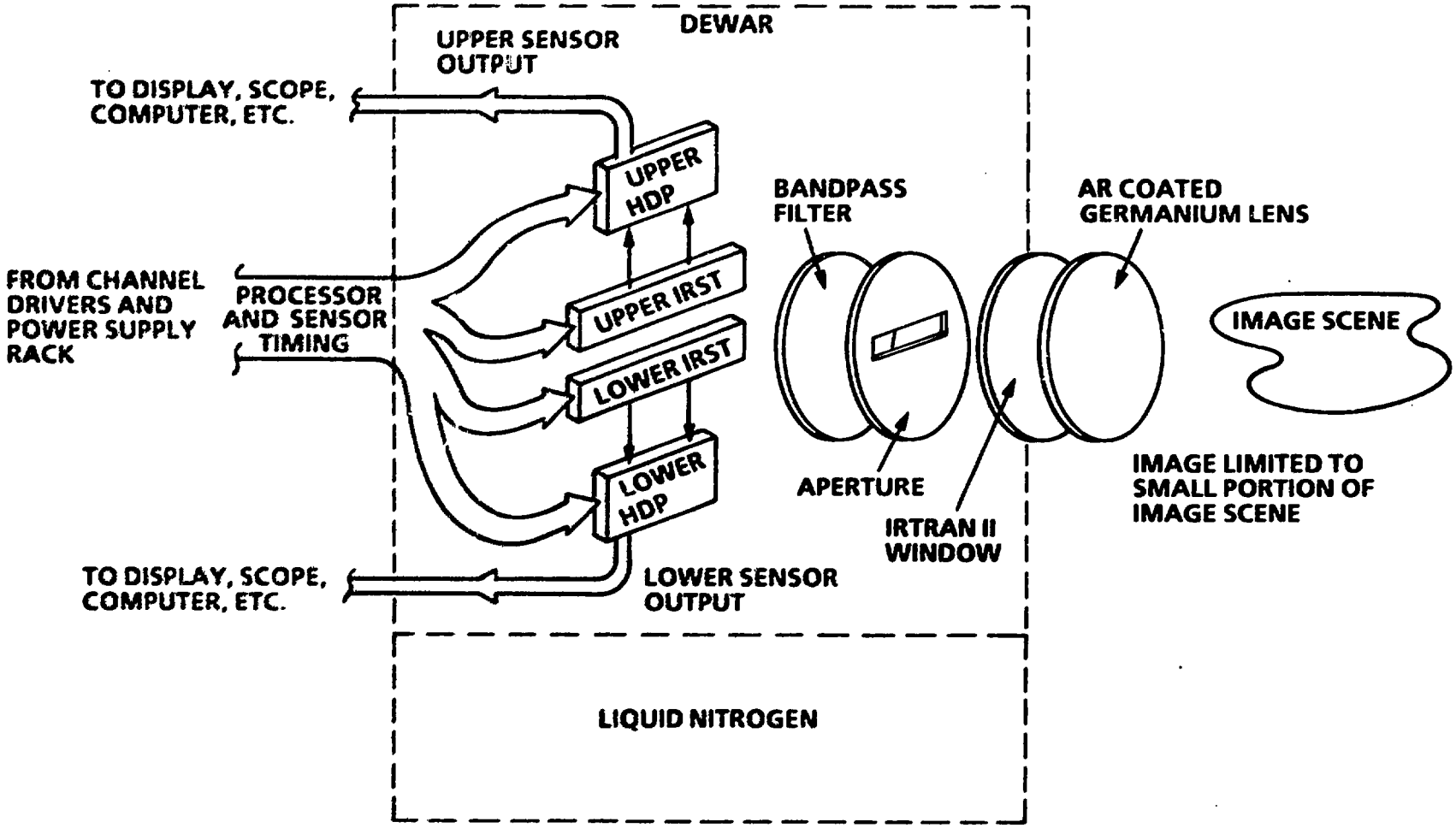


Figure 6-11. Dewar/CIM/HDP (nonscanning) optics diagram.

Lens, aperture, and filter selection are critical for achieving the required fields of view and background flux densities at the detector array. The aperture plate, as shown in the figure, is placed between the imaging lens and bandpass filter, and contains a rectangular aperture with an approximate 8:1 aspect ratio. This configuration provides near-uniform illumination across the array (with minimal vignetting of the far-field scene) and also minimizes the near-field component of the total background flux. Several plates were fashioned, with apertures ranging from 4.6×37 mm to 5.2×42 mm, to provide a limited range of background flux densities and fields of view.

The IR lens is an antireflection-coated, 2-inch-diameter germanium lens of 200-mm focal length ($f/4$). An Irtran II window is placed between the lens and aperture plate and is vacuum-sealed to the dewar lid. Since stray or near-field radiation degrades the imaging quality of any sensor, the IR bandpass filter was placed as close as possible to the detector surface using the specially designed holder described previously, which also provides an efficient thermal sink for the filter. The complete arrangement is shown in Figure 6-12, which is the same as Figure 6-4 rotated 90 degrees about the dewar axis to show the long dimension of the CIM array and cold-shield aperture.

If larger fields of view are desired, the present filter/aperture configuration would need to be modified. Since layered-dielectric filters are extremely costly in diameters greater than 1 inch, an attractive alternative is an AR-coated single-element silicon filter. These are produced commercially in 2-inch-diameter wafers that can easily be sawed to smaller sizes, are significantly less costly (about $90 each in small quantity), and, thus, may be treated expendably. The IR transmission characteristics of the two types of filter are similar, as shown in Figure 6-13, with only a small penalty in average IR transmission over the 8- to 10-μm band (about 5 to 10%) realized with the coated-silicon filter.

Imaging of the linear IRST array(s) could be achieved with the present system by integration of an electrically driven mechanical scan mirror between the image scene and the IR lens. The scanner rotation would be made synchronous with the clocking of the CIM array to produce a two-dimensional focal-plane image. This modification was not implemented on the present program effort.

E. TEST EVALUATION

The LN_2 dewar module and test electronics were verified using prequalified HDP pairs mounted in 96-pin packages with calibrated temperature sensing diodes in various locations. Cooldown tests verified that the device package reached stable LN_2 testing temperatures within 10 minutes, while the IR filter platform attained an adequate cold-shielding temperature of 90 K within approximately 1 hour. With a full CIM FPA running (and each HDP dissipating about 70 mW power), it would be necessary to pump over the LN_2 reservoir to achieve operating temperatures of 77 K and below, and temperature stabilization could take significantly longer.

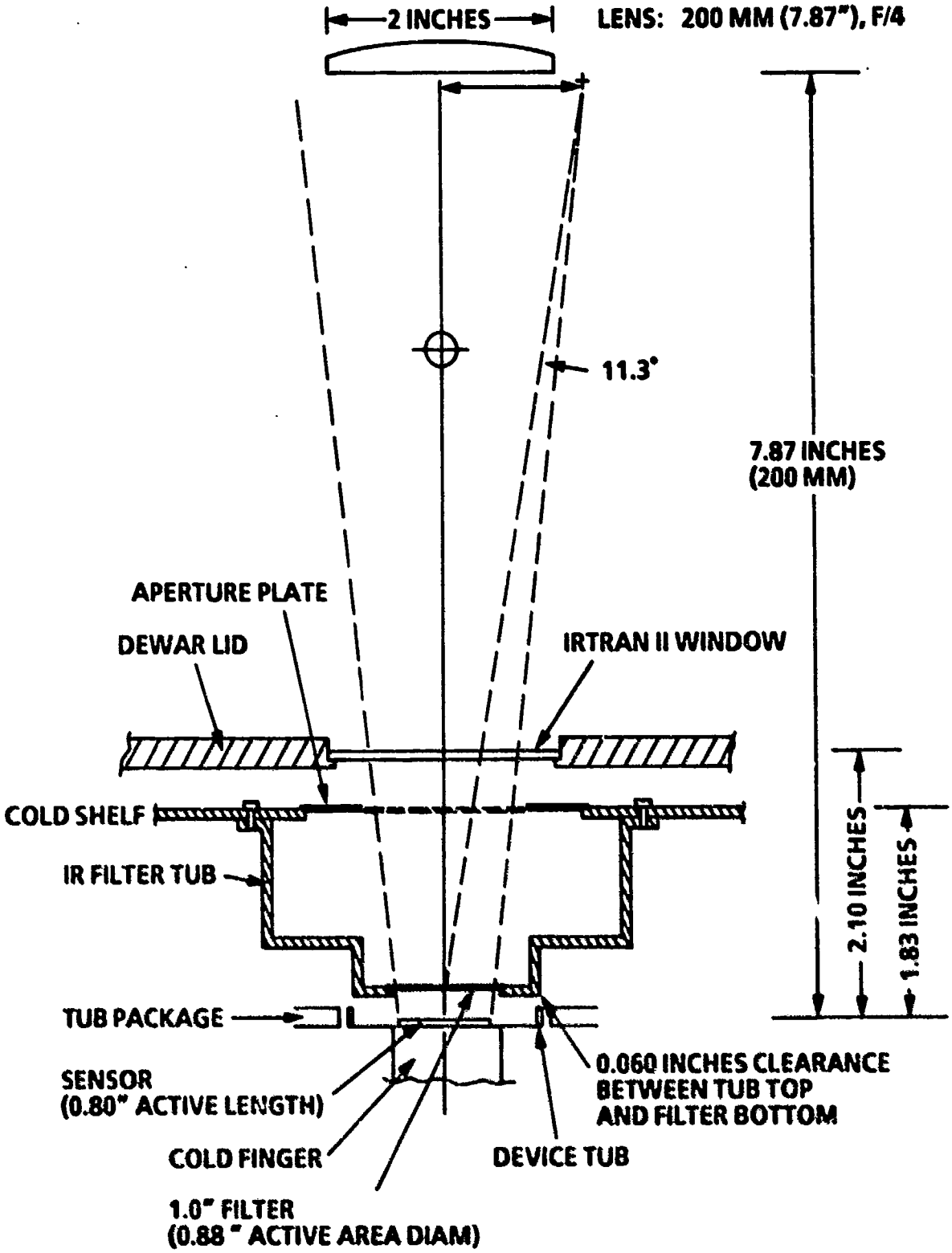


Figure 6-12. Cross section of cold-shield configuration and system optics, viewed perpendicular to long dimension of CIM array and aperture.

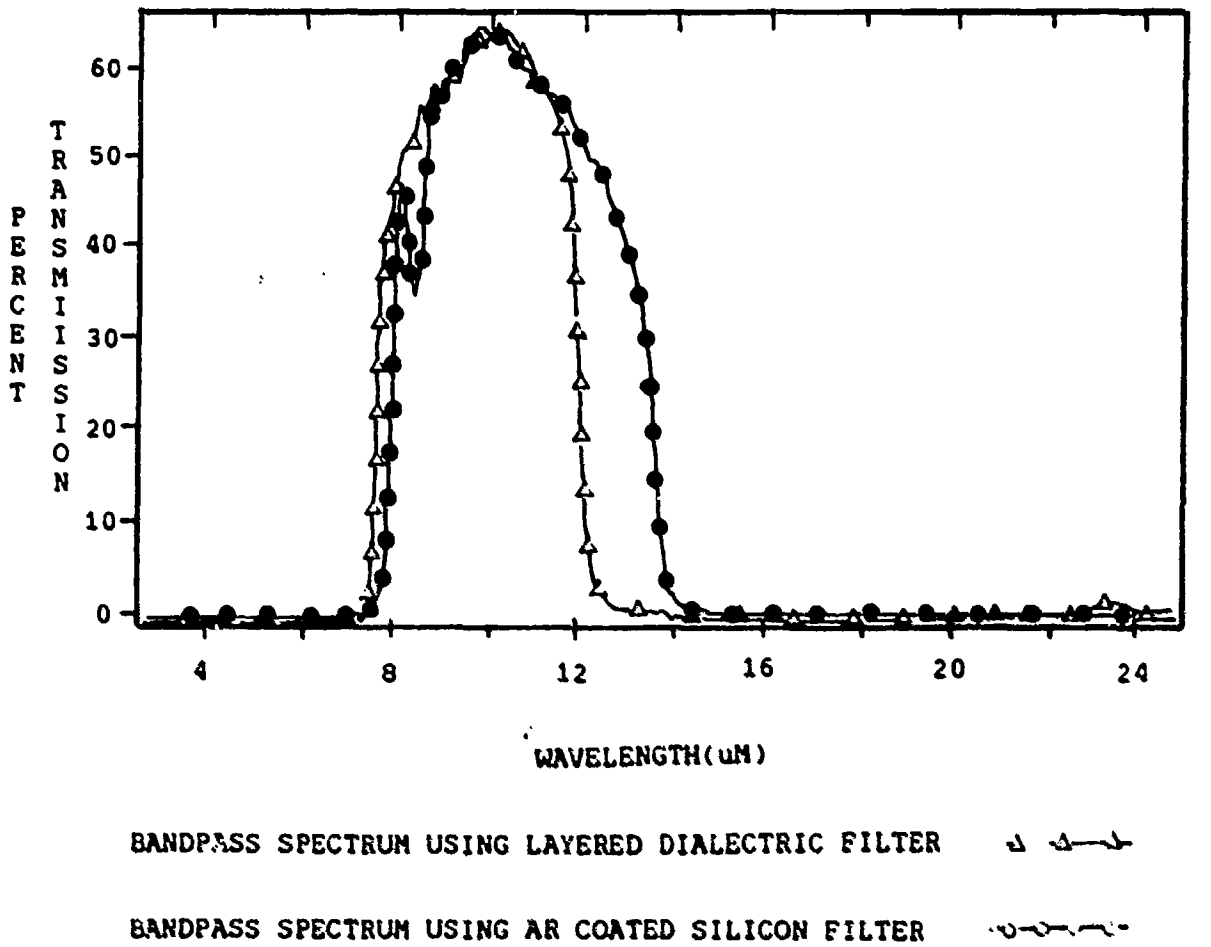


Figure 6-13. IR bandpass spectra of AR-coated silicon filter and layered-dielectric filter.

Results of initial processor testing (without a CIM array installed), summarized in Table 6-1, confirmed all dewar electronics and verified that the focal-plane-mounted HDPs operated very near expected performance levels. Testing of subsequent processor pairs confirmed these initial results, and quantitative variations in HDP performance were small. A typical timing pattern used to drive the HDPs is shown in Figure 6-14. These patterns are similar to those used with other CIM devices, notably the large-area CIM, but suitably scaled to the shorter MIS integration times and higher data rates appropriate to LWIR CIM detectors.

Although the optical system could not be fully evaluated without a CIM array in place, the IR bandpass characteristic of the composite filter/window assembly was measured and the result used in calculations of background flux densities to verify that these met system operating requirements. The measured IR transmission spectrum (at room temperature) of the cold-shield bandpass filter is shown in Figure 6-15. The external optics are of standard design and construction and required no special testing.

Table 6-1. HDP Test Results

Operating Conditions			
HDP Substrate:	-2.0 Vdc	VB1:	2.5 Vdc
VDD:	14.0 Vdc	VC:	4.3 Vdc
VSC:	3.2 Vdc	VB2:	2.0 Vdc
HDP Driver:	10.0 Vdc	V (R):	1.35 Vdc
VSC2:	4.3 Vdc		

Device Temperature = 81 K
Filter Temperature = 87 K

Test Results	Predicted	Actual
HDP preamplifier gain	25	21
Overall processor gain	18	14
Channel input reference noise (channel = 0.0 Vdc)	10.5 μV rms	13 μV rms

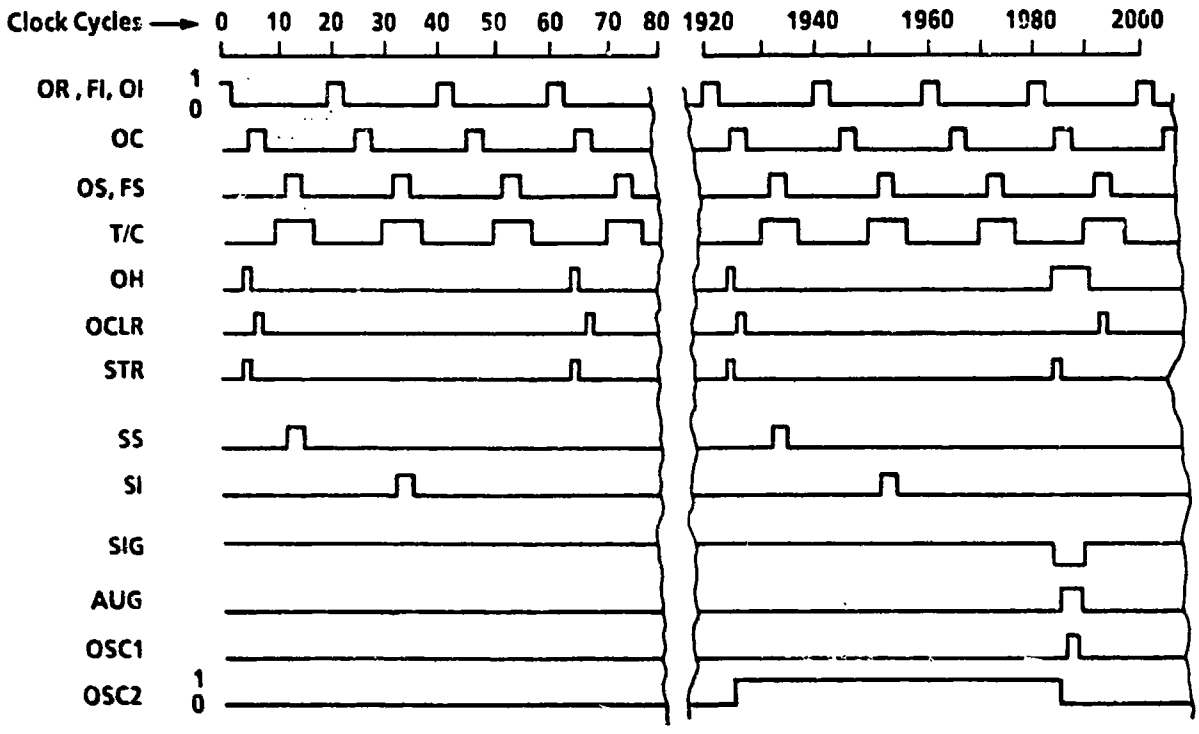


Figure 6-14. Typical IRST/HDP timing-sequence schematic.

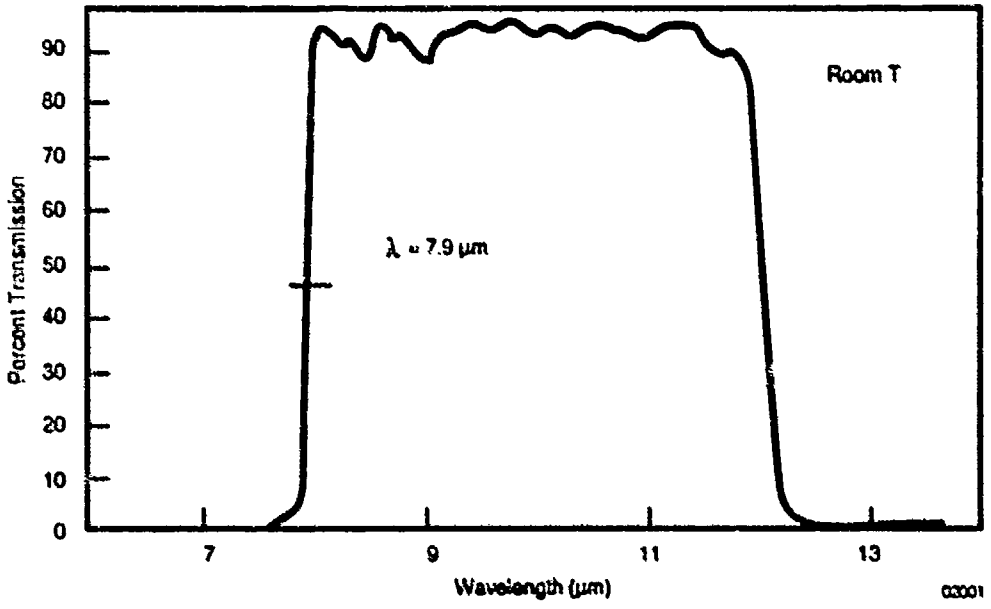


Figure 6-15. IR transmission spectrum of IRST cold-shield bandpass filter assembly.

SECTION VII
ARRAY SCREENING AND CHARACTERIZATION

A. DEVICE SELECTION

CIM arrays for focal-plane screening and performance evaluation were selected from IRST Lot 8B, the first lot fabricated on LWIR material with high process yield. A summary of room-temperature probe data for Lot 8B is given in Section IV and repeated in Table 7-1. All arrays were of the TDI type and standard (nonvertically integrated) configuration; five were on SSR HgCdTe and two on LPE. All demonstrated high detector row yields; only one array (048) exhibited interlevel electrical defects, and one array (037) had a shorted field plate.

Table 7-1. Probe Yield Summary for IRST Lot 8B

Array	Type	Substrate Material	Field Plate	Transfer Gate Left	Transfer Gate Right	Row Shorts to Substrate	Row Shorts to FP or TG	Net Row Yield (%)
037	TDI	SSR	Short to substrate	Good	Good	0 of 16	0	100
044	TDI	SSR	Good	Good	Good	1 of 16	0	94
045	TDI	SSR	Good	Good	Good	0 of 16	0	100
046	TDI	SSR	Good	Good	Good	0 of 16	0	88
048	TDI	SSR	Good	Good	Good	0 of 16	2	88
080	TDI	LPE	Good	Good	Low capacitance	1 of 16	0	94
081	TDI	LPE	Good	Good	Good	0 of 16	0	88*

* Two rows shorted together

Following probe, arrays were separated from their test-structure strips and permanently mounted and bonded to the custom ceramic carriers described in Section VI.C and shown in Figure 6-7. (The carriers, designed for the 480 × 1 linear CIM, can accommodate the slightly wider TDI array but allow only 8 of the 16 rows to be bonded and tested.) These in turn were mounted in temporary fashion in standard 40-pin test packages for low-temperature MIS and diode screening, as shown in Figure 7-1; test structures were similarly mounted (in permanent fashion) in separate packages. Use of the ceramic carriers in this fashion permitted direct evaluation of CIM MIS and diode characteristics without need for additional bonding on the HgCdTe. An array selected for subsequent performance evaluation had its carrier removed from the test package and mounted directly in the composite focal plane carrier (Figure 6-9), where the ceramic leads were then wire-bonded to those of the outboard silicon processor chips.

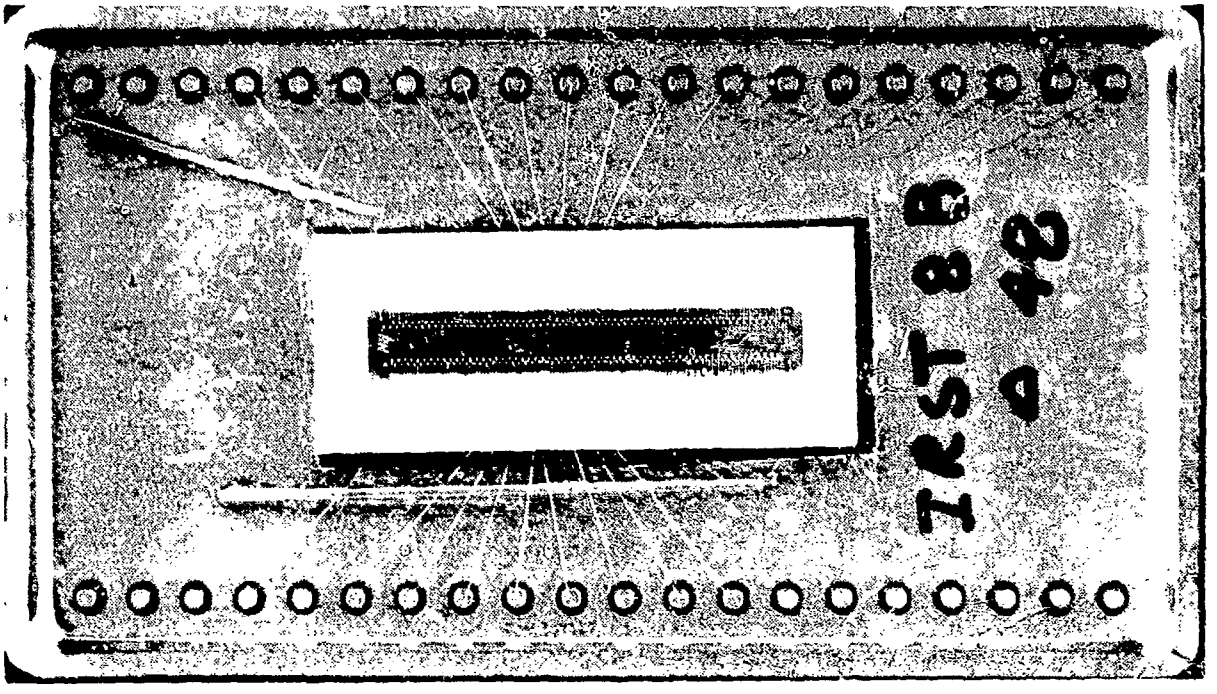


Figure 7-1. 480 × 4 IRST array and ceramic carrier mounted in 40-pin test package for MIS and diode screening.

Of the arrays tested, 8B-080 and 8B-081 had superior MIS and diode characteristics and were selected for further evaluation. Of the two, array 8B-081 demonstrated superior row-and-column CIM performance at both 77 K and 65 K, and this array was chosen for the final program deliverable. All screening data presented in this section were obtained on these two arrays, and all performance data presented were obtained on the deliverable focal plane, 8B-081.

B. MIS AND DIODE SCREENING

A pinout diagram of the 40-pin test package is shown in Figure 7-2. The package permits pinout of 8 of 16 detector rows, plus field plate, transfer gates (TG and RG), and 27 randomly selected diode outputs from both sides of the array (with two pins reserved for substrate). Before testing, all samples received a 60 °C bake of at least 4 hours duration to ensure uniformity of MIS flatband voltages following UV exposure during assembly and bonding. Screening measurements were performed at both 80 K and approximately 62 K, the lower temperature achieved by pumpover of the dewar nitrogen reservoir and confirmed by means of a calibrated sense diode fixed to the test package.

Typical MIS capacitance-voltage curves for a single row of detectors at both operating temperatures and 0 degree FOV are shown in Figure 7-3. At 80 K, C-V response is nearly low-frequency in character, although still clearly p-type. At 62 K, response is nearly high-frequency and

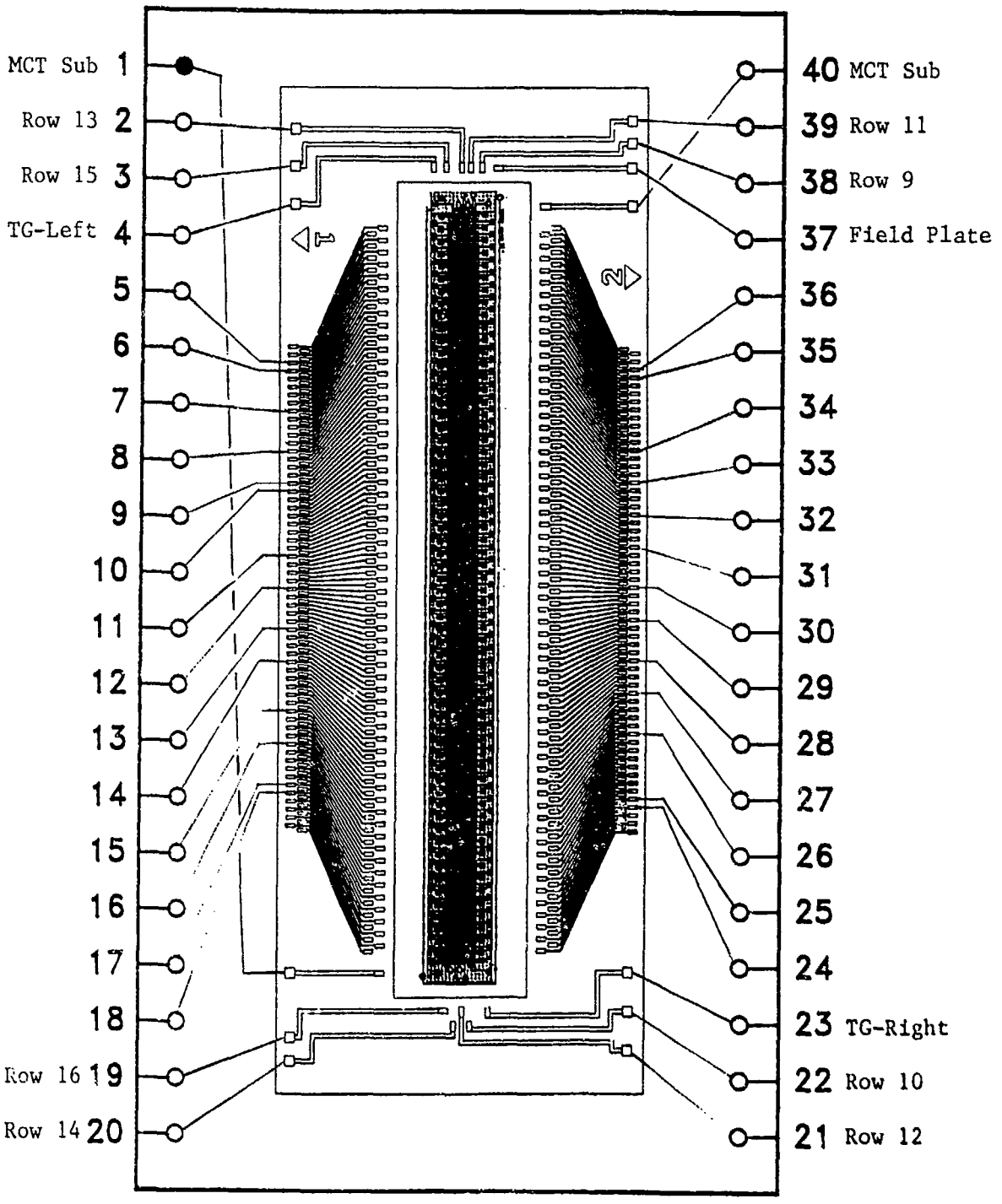


Figure 7-2. Pinout diagram of 40-pin test package with IRST array.

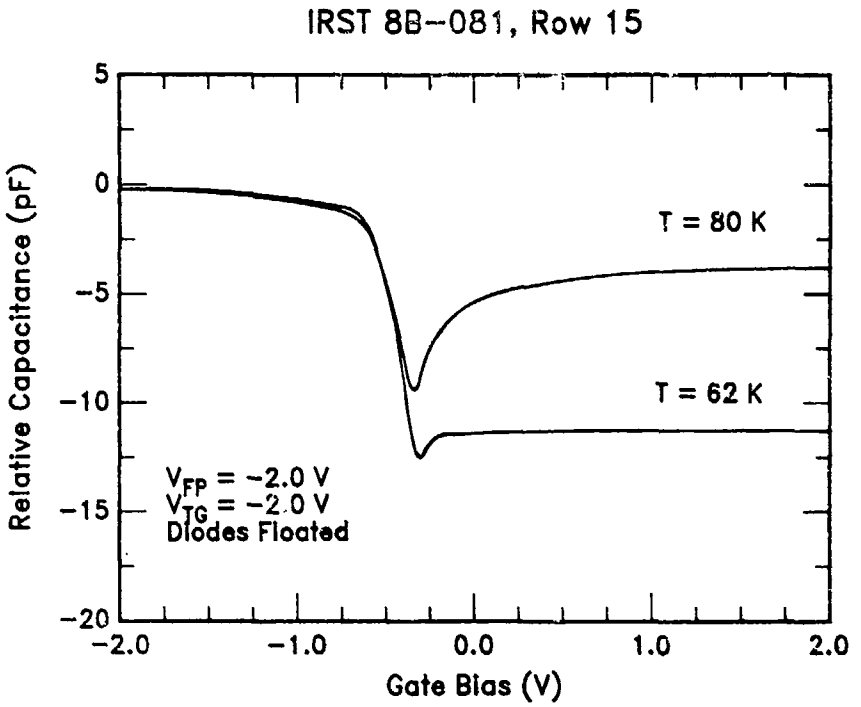


Figure 7-3. 1-MHz capacitance-voltage curve at two operating temperatures for single row of detector elements of IRST 8B-081.

indicates an effective acceptor concentration ($N_a - N_d$) of about 7.5 to 10×10^{14} cm^{-3}. In both cases, the CIM field plate and transfer gate were maintained at –2 V bias to accumulate the surface regions outside the detector gates. (With anodic-sulfide passivation, both field-plate and transfer-gate regions have MIS flatband voltages between –0.5 V and –1.5 V relative to substrate.) C-V response was uniform among the eight rows tested.

MIS charge-storage capability was evaluated under 0-degree FOV by operating the entire CIM row as an MIS detector (with field plate and transfer gate accumulated), using the test circuit shown schematically in Figure 7-4. No measurable charge storage was observed at 80 K, consistent with the low-frequency C-V character at this temperature. At 62 K, dark storage times of 75 to 250 μs were obtained, as illustrated for one row in Figure 7-5. The row shown had net storage time of –180 μs and 50% storage time (the time to half-full well, a more meaningful measure of usable storage capacity in detector operating mode) of 50 μs, more than adequate to meet IRST operating requirements at this temperature. The 50% storage time for the worst row measured was ~15 μs, still adequate to permit detector integration times of 5 to 8 μs.

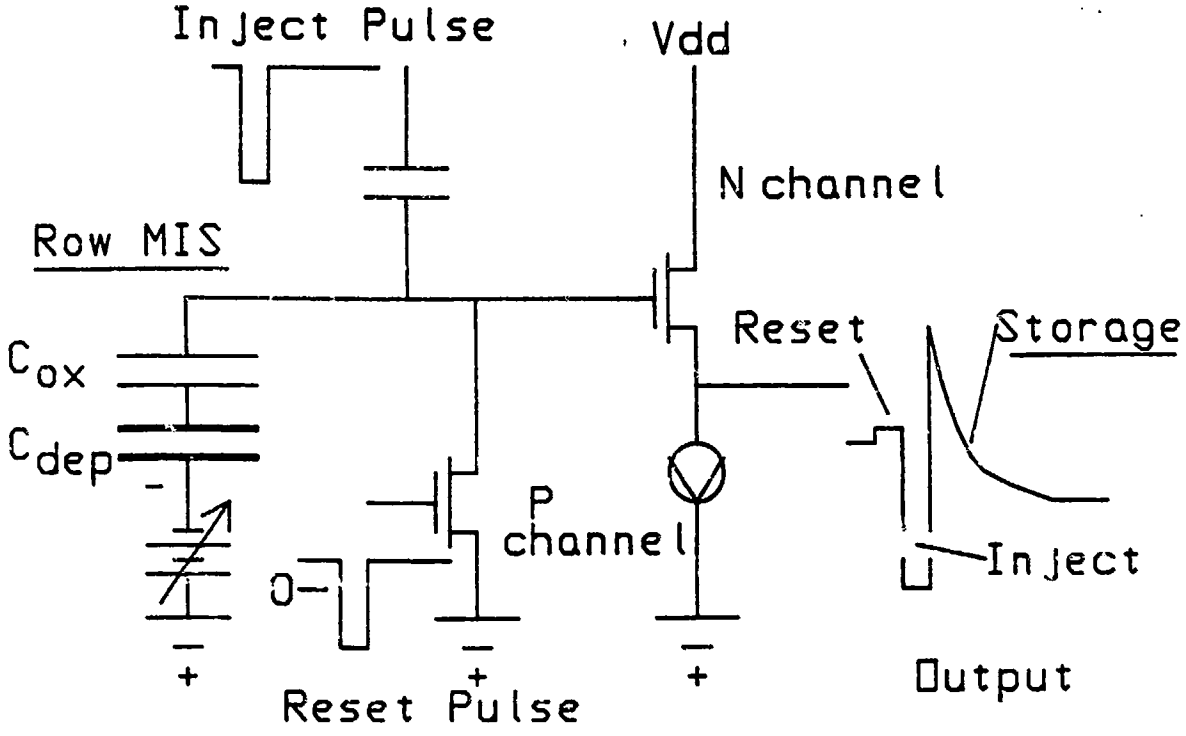


Figure 7-4. Diagram of test circuit for determining MIS storage times of CIM rows.

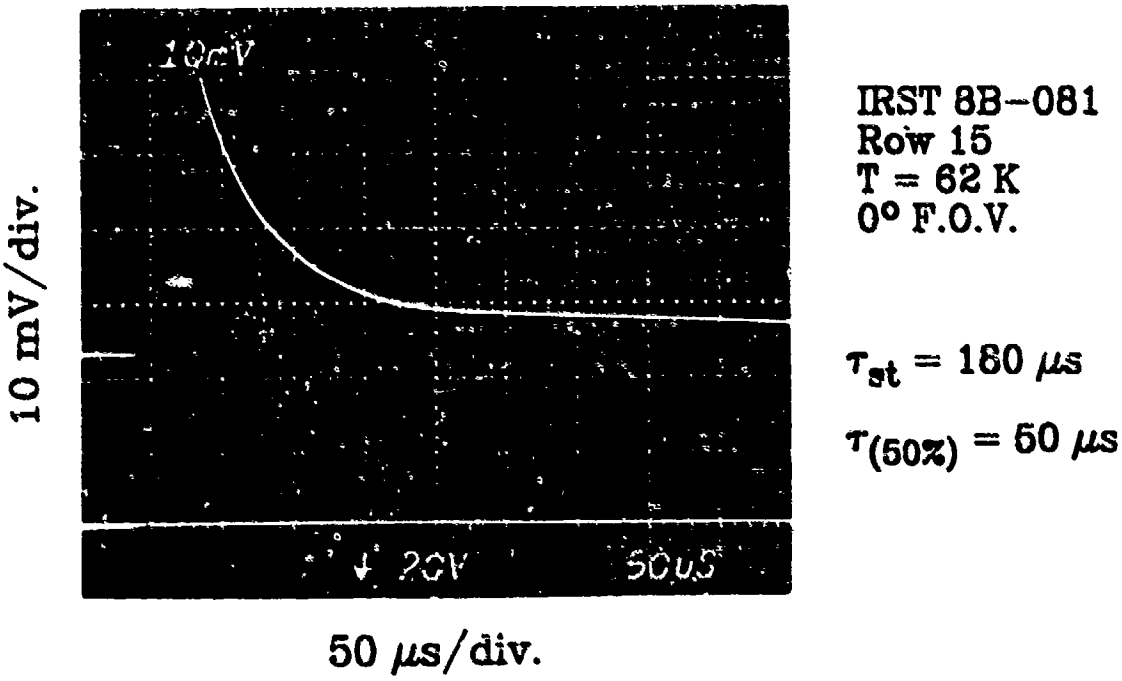


Figure 7-5. MIS charge-storage characteristic for one row of IRST 8B-081 at T = 62 K and 0-degree FOV.

Diode current-voltage characteristics were also measured at 80 K and 62 K. Results for two diodes of 8B-081 are shown in Figures 7-6 and 7-7, and represent near-best and near-worst cases among the 27 diodes sampled. In the best case, lowering the operating temperature to 62 K produces a two-order-of-magnitude reduction in leakage current out to 0.4-V reverse bias and an order-of-magnitude reduction even at 0.7 V. In worst case, the reduction varies between a factor of 2 and 4 over the same range of bias, and the leakage current at 80 K is not significantly higher than for the best case.

To measure these results against CIM performance requirements, the corresponding leakage-current densities at 0.5-V reverse bias were calculated for all diodes tested. Results for arrays 8B-081 and 8B-080 are summarized in Table 7-2. The IRST performance predictions presented in Section II.D assumed a maximum leakage-current density of 5 mA/cm^2, which, for the TDI diode geometry, corresponds to a net current of approximately 300 nA. At 80 K, all 27 diodes on both arrays exceed this leakage limit. At 62 K, 92% (on 8B-081) and 82% (on 8B-080) satisfy the requirement; on 8B-081, in particular, nearly half the diodes tested had leakage currents at least an order of magnitude smaller than the 300-nA limit. (The distribution could be improved further by choosing a lower reverse bias voltage.) Since the diodes were selected at random (and with roughly equal spacing), these results are considered to represent a statistical sampling of the 240 CIM output diodes.

The effect of field-plate bias on diode characteristics was examined using single-element

Table 7-2. Diode Leakage Distribution for IRST Lot 8B

			No. With Leakage Current in Specified Range at 0.5-V Reverse Bias			
Array	Temperature	No. Diodes Sampled	< 30 nA	30 to 300 nA	300 nA to 3 μA	> 3 μA
8B-081	80 K	27	0	0	26	1
	62 K	25 (2 open)	12	11	1	1
8B-080	80 K	27	0	0	8	19
	62 K	27	0	22	4	1

CIM test structures having the same diode and pixel configuration as the array itself. Results at 80 K and 62 K are shown in Figure 7-8. Biasing the field plate into deep depletion or inversion ($V_{FP} > 0$) produces a fairly uniform increase in leakage from 0 V to about 0.6 V reverse bias at both temperatures, with a greater increase at the lower temperature as expected. Biasing the field plate into accumulation ($V_{FP} < 0$) produces no change in leakage for small reverse bias (< 0.2 V) but an exponential increase at higher bias levels. This behavior is also expected and arises from the field-induced junction formed under the field plate at negative gate bias, as described in Section III.D. This

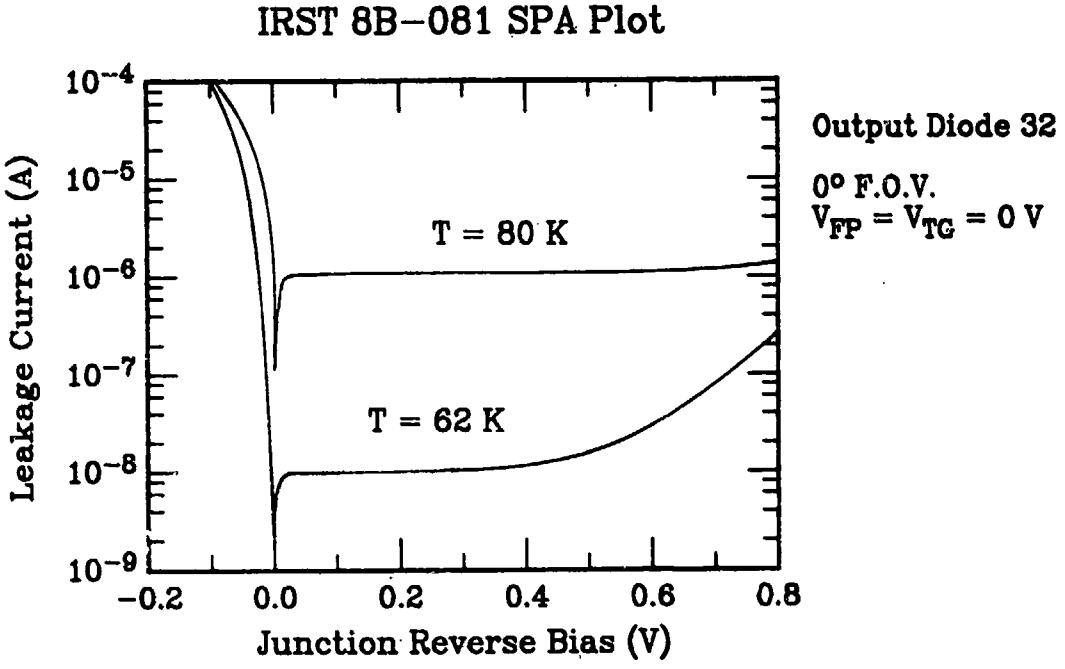


Figure 7-6. Current-voltage (I-V) curve at two operating temperatures for one output diode of IRST 8B-081, representing a near-best case of 27 diodes tested.

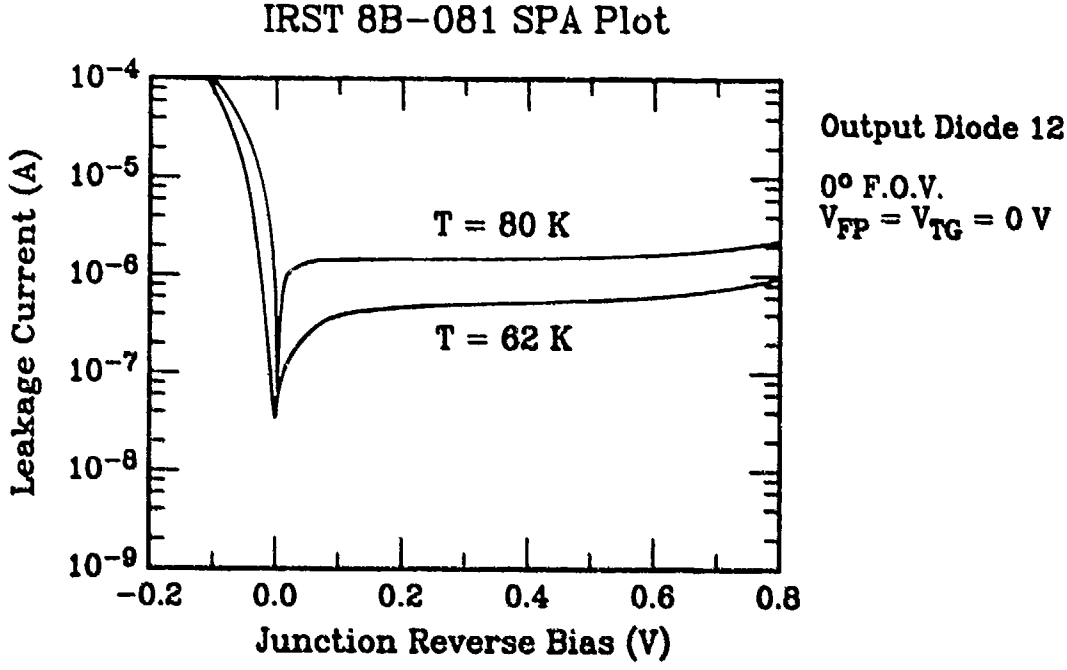
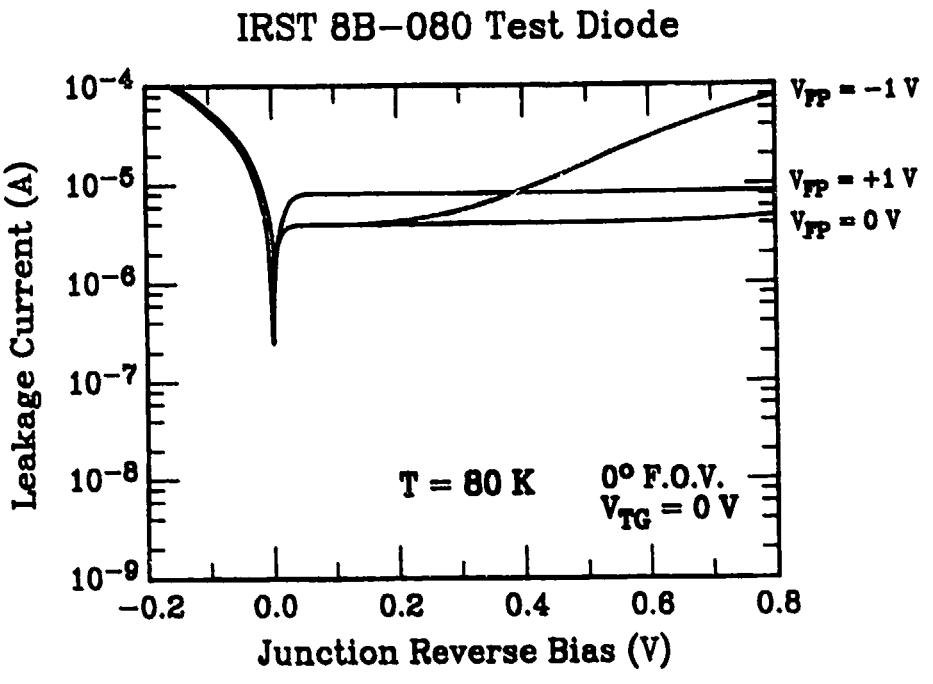
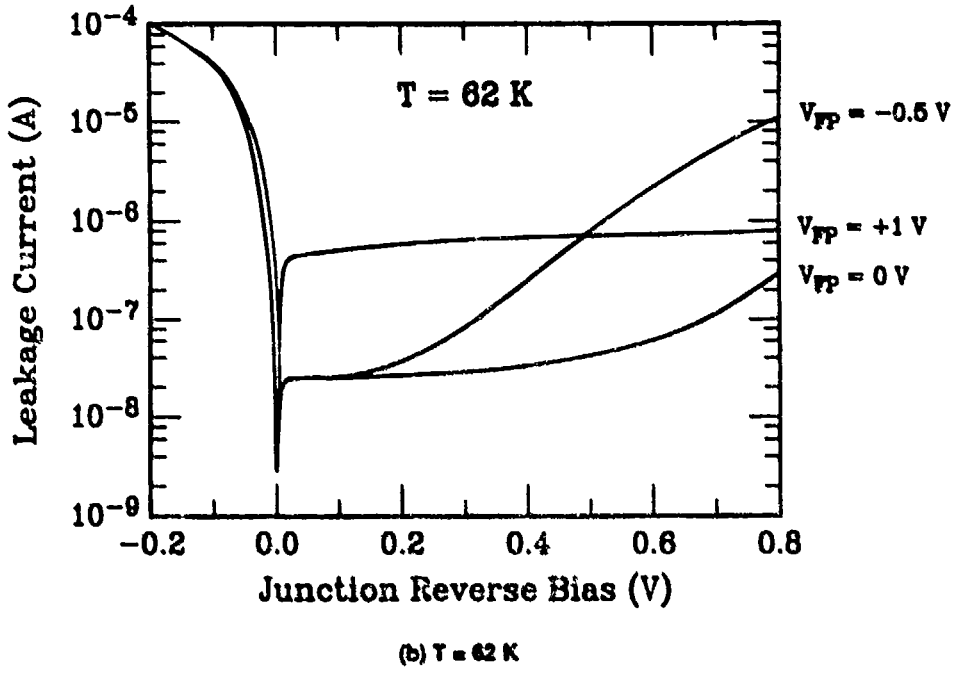


Figure 7-7. Current-voltage curve at two operating temperatures for one output diode of IRST 8B-081, representing a near-worst case of 27 diodes tested.



(a) T = 80 K



(b) T = 62 K

Figure 7-8. Effect of field-plate bias V_{FP} on current-voltage characteristics of a diode test structure from IRST 8B-080.

effect is more pronounced at the lower temperature, where a field-plate bias of –0.5 V produces an order-of-magnitude increase in leakage at 0.5 V reverse bias. At both temperatures the diode I-V curves were essentially unchanged for field-plate biases between 0 V and +0.2 V.

All MIS and diode measurements on 8B-081 and 8B-080 were performed without benefit of a high-temperature (100°C) anneal, which could be expected to further improve diode and MIS characteristics. Since these were the first functional IRST arrays, however, and since the postanneal is aimed primarily at improving diode noise performance, we decided to forego annealing until after initial performance evaluations.

C. IR SPECTRAL RESPONSE

IR spectral response was determined by measuring the modulation of the CIM row capacitance (in depletion at 80 K) by an incident IR signal in the 6- to-12-μm band, using a Mattson FT-IR spectrometer. Figure 7-9 shows results for array 8B-081. The response curve shows near-classical behavior from the lower spectral limit out to about 9.3 μm, with an effective cutoff (50% response point) at about 9.8 μm. With this technique, any variations in cutoff wavelength along the array (arising from nonuniformities in substrate composition) are averaged and result in a softer spectral edge, reflecting the distribution of cutoffs among the pixels sampled. (The spectrometer spot size is –0.5 in., and samples about two-thirds of the pixels in a given detector row.) Spectra obtained from five rows across the width of the array, however, showed a maximum variation in effective cutoff of only 0.03 μm.

Figure 7-10 is the IR response for one row of array 8B-080. Measured cutoff was about 10.5 μm, with the trailing edge of the distribution extending beyond 11 μm. Spectra for three other rows of the array measured were indistinguishable from the one shown, with 50% response occurring at 10.45 μm in all cases.

Spectral-response measurements were made with the absence of an IR cold-shield filter. Subsequent array performance evaluations were conducted with an integral cold-shield filter having a lower bandpass limit of 7.9 μm.

D. DETECTOR PERFORMANCE

Following screening and spectral-response measurements, array carriers were removed from the 40-pin test packages (which required removal of bond wires from the carrier leads only) and assembled with a pair of prequalified Si HDP processors on the IRST composite carrier (Figure 6-6). The composite assembly was then mounted and bonded in a standard 96-pin test package for performance evaluation in the dedicated CIM dewar. A completed example is shown in Figure 7-11.

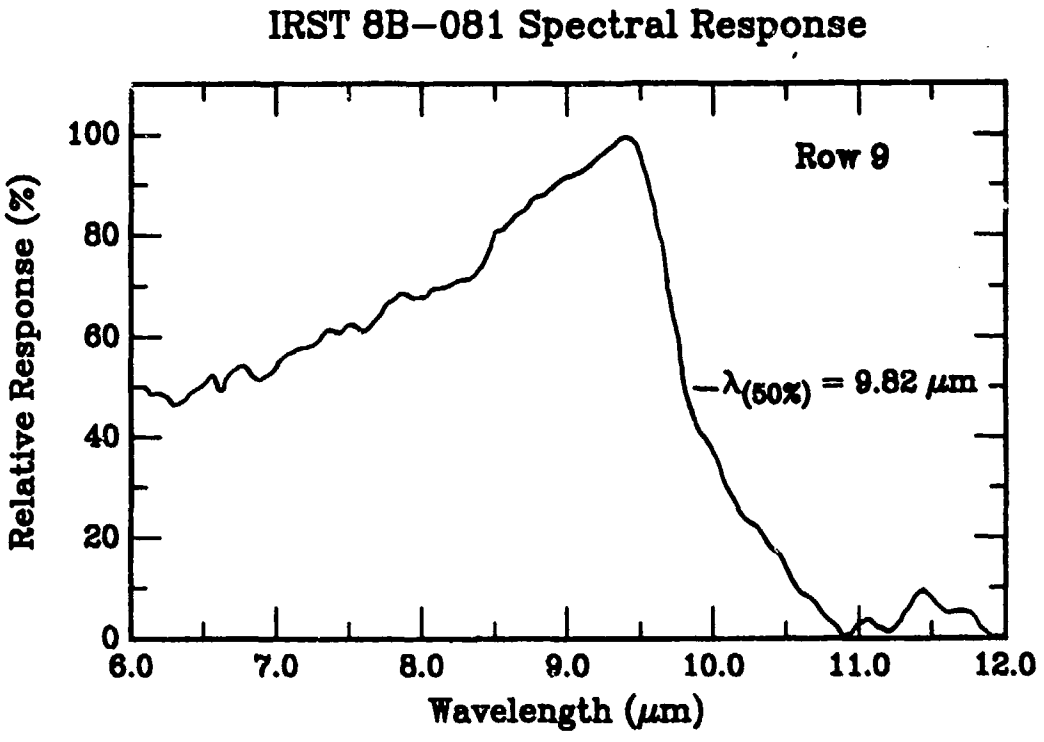


Figure 7-9. IR spectral response of IRST 8B-081.

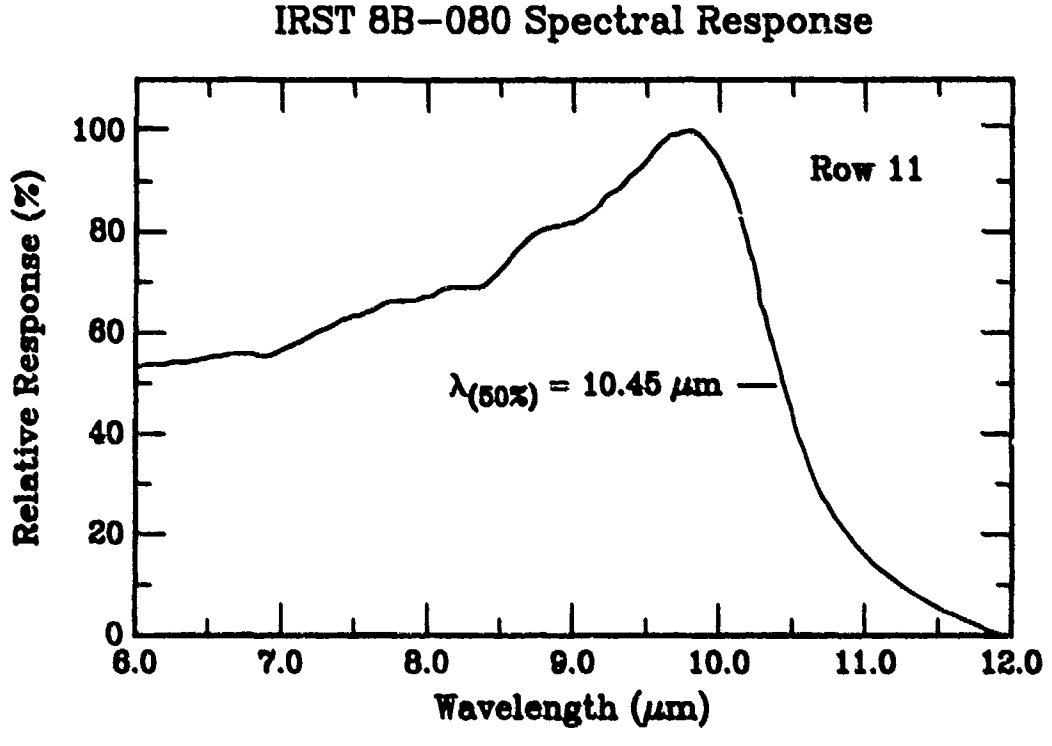


Figure 7-10. IR spectral response of IRST 8B-080.

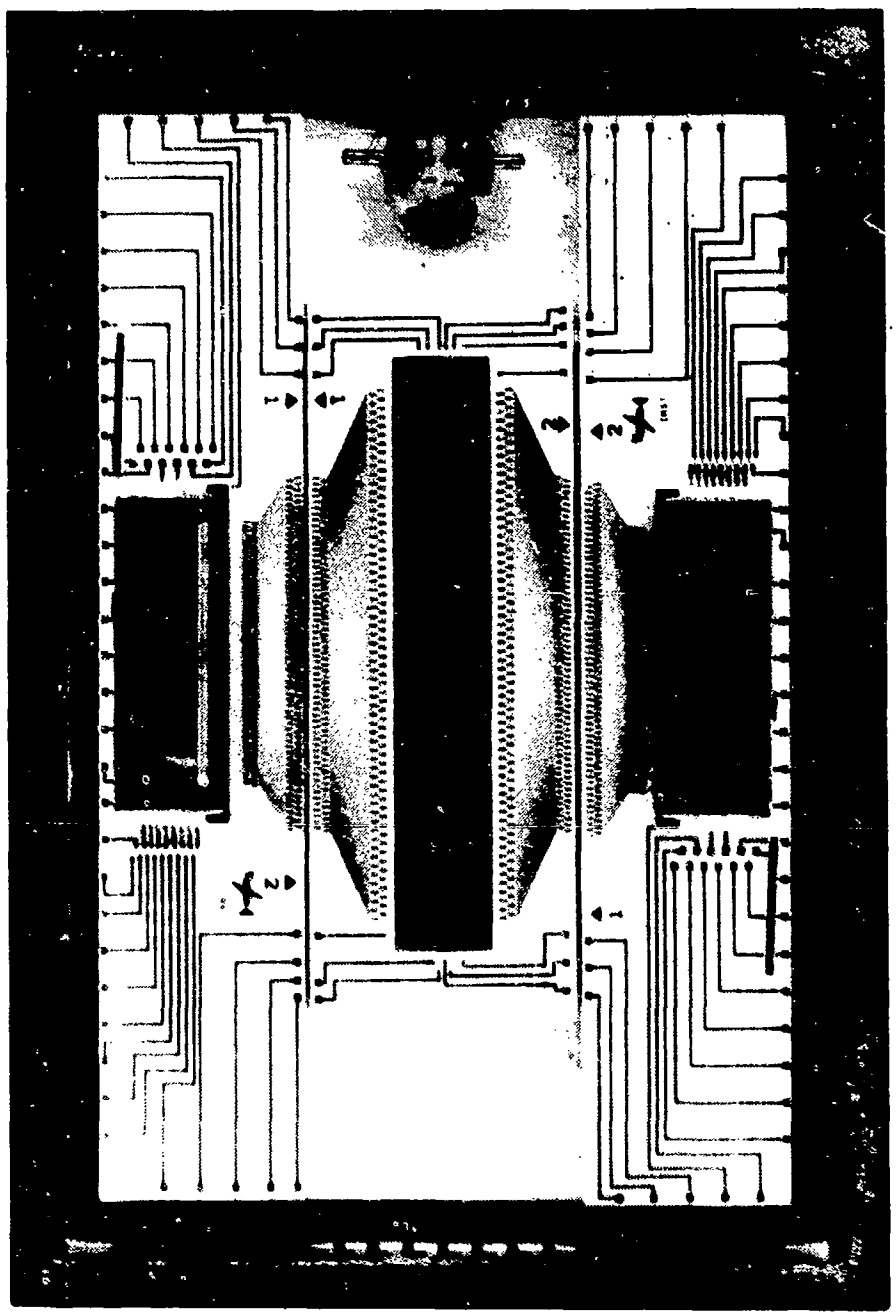


Figure 7-11. Composite focal-plane assembly in standard 96-pin test package for performance evaluation.

Of the two Lot 8B arrays tested in this configuration, 8B-081 showed superior performance at both liquid-nitrogen and reduced temperatures. Minimum operating temperature (with nitrogen pumpover) was approximately 65 K, 5 K higher than the dewar coldfinger because of heat loading from the Si HDPs, which dissipate about 80 mW power each. This temperature could be maintained for 3 to 4 hours of testing without depleting the nitrogen reservoir. Operating temperature without pumpover was 80 K to 82 K and could be maintained indefinitely.

Detector responsivity was measured using a chopped blackbody source at 900 K. Figure 7-12 is a plot of signal voltage (processor-output referred) versus signal flux for a typical detector element of 8B-081 at T = 65 K with *f*/3 optics. The plotted signal flux assumes an extrapolated IR cutoff at 65 K of 10.1 μm (from 9.8 μm at 80 K). Detector integration time was 4 μs and background flux at this FOV (limited by optics transmission and the spectral bandpass of the coldshield filter) was 5×10^{15} ph/cm^2 s. Under these operating conditions, response was linear out to 3×10^{16} ph/cm^2 s, satisfying the IRST design goal for a detector cutoff of 10 μm.

The corresponding single-pixel responsivity may be calculated approximately as

$$R_{V/W} = \frac{V_{sig}}{\Phi_{sig} A_{op}} \bullet \frac{\lambda_p}{hc} \qquad (7-1)$$

where A_{op} is the pixel active area, V_{sig}/Φ_{sig} is the slope of the response curve in the linear regime, and hc/λ_p is the average energy per incident photon near peak response. (From Figure 7-9, $\lambda_p \sim 9.5$ μm, extrapolated to 9.8 μm at 65 K.) From the data of Figure 7-12, the calculated responsivity for this detector element is $R_{V/W} = 63$ MV/W, output referred. For a processor gain of approximately 10, this yields a responsivity at the CIM output of about 6 MV/W.

At 65 K, the array could be operated at integration times up to 10 or 12 μs with good performance. Figure 7-13 compares linearity data for 4-μs and 10-μs integration for the same detector element of the previous figure. At 10 μs, the response begins to deviate significantly from linearity above about 1.5×10^{16} ph/cm^2 s, but does not saturate completely even at the highest flux levels measured. The ratio of responsivities for small signal flux, which ideally should equal the ratio of the respective integration times (2.5), is approximately 1.8. For 10-μs integration, $R_{V/W} = 110$ MV/W (output referred).

The same array was subsequently operated at 80 K with reasonable performance. Figure 7-14 shows single-pixel linearity data for integration times of 4, 6, 8, and 10 μs at the higher operating temperature. (Here, the plotted signal flux is based on the measured cutoff at 80 K). Output signal at low flux levels ($< 0.5 \times 10^{16}$) for 4-μs and 10-μs integration is the same as at 65 K (Figure 7-13), as expected. At higher flux levels, the signal begins to saturate, more rapidly for longer integration time, and the saturation level decreases with increasing integration time.

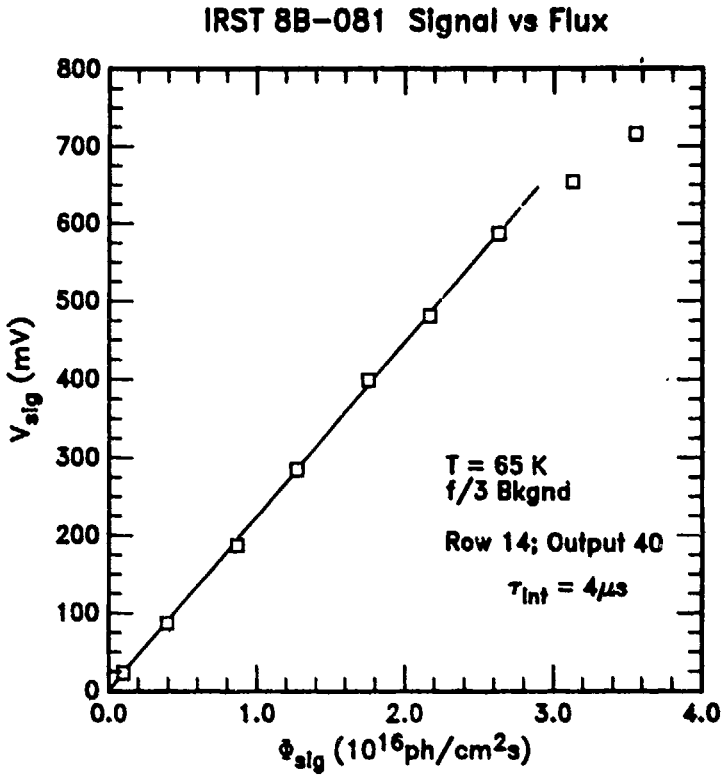


Figure 7-12. Response versus 900 K signal flux for typical detector element of IRST 8B-081 at T = 65 K and *f*/3 FOV. Integration time was 4 μs. Corresponding single-pixel responsivity is 63 MV/W (output referred).

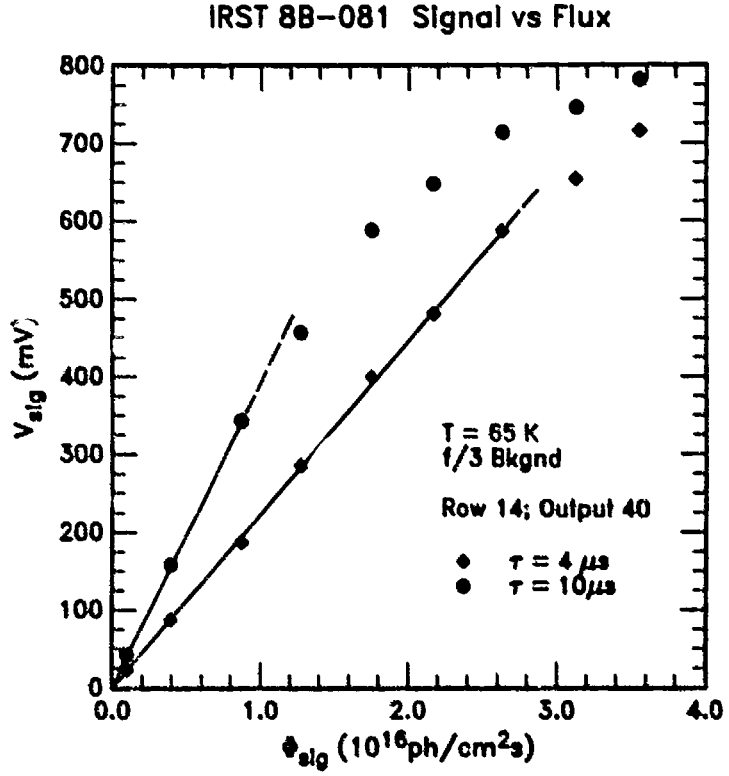


Figure 7-13. Responsivity data for same detector element of Figure 7-12 for two different integration times. (T = 65 K).

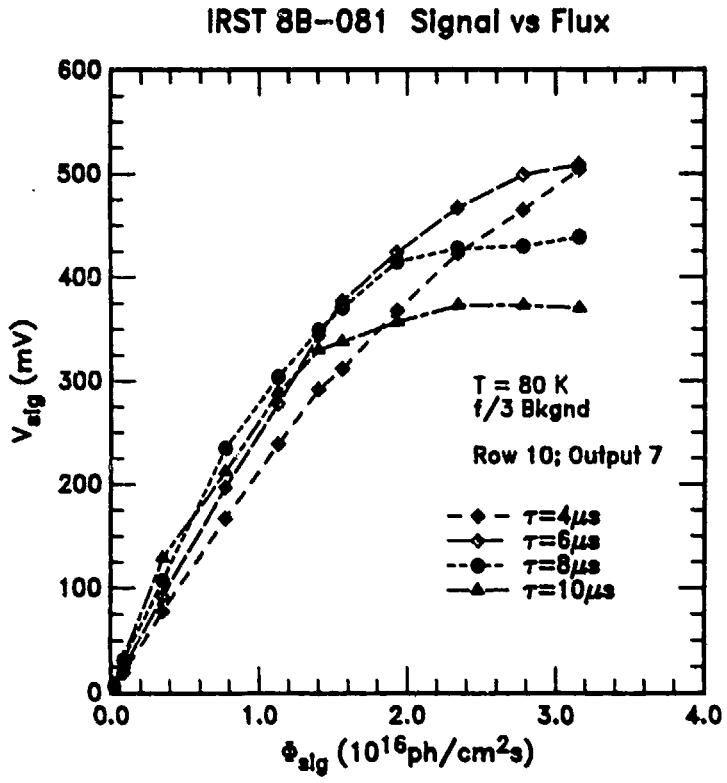


Figure 7-14. Responsivity data for typical detector element of IRST 8B-081 at T = 80 K and four different integration times.

This behavior is explained by the simple CIM model. The detector response to a chopped blackbody signal is proportional to the difference in total integrated charge with the blackbody shutter opened versus closed. With the shutter closed, both background-generated and dark charge collect in the MIS well; after an integration time τ_i, the total accumulated charge is:

$$Q_{closed} = \Phi_B A_{op} \eta q \tau_i + \overline{j_D} A_{st} \tau_i \qquad (7-2)$$

where Φ_B is the background flux, j_D is the average MIS dark current for the given pixel, A_{st} is the total storage area (transparent plus opaque) of the detector gate, η is the quantum efficiency, and q the electronic charge. With the shutter open, the total charge collected is:

$$Q_{open} = \Phi_{sig} A_{op} \eta q \tau_i + \Phi_B A_{op} \eta q \tau_i + \overline{j_D} A_{st} \tau_i \qquad (7-3)$$

where Φ_{sig} is the signal flux. The net signal charge Q_{sig} is then the difference of the two, or just $\Phi_{sig} A_{op} \eta q \tau_i$. However, Q_{open} cannot exceed the MIS full-well capacity $Q_{FW} = C_i \Delta V$, where C_i is the gate insulator capacitance and ΔV is the bias past threshold. Thus, the net signal charge collected cannot exceed the maximum value

$$Q_{sig}^{max} = Q_{FW} - \left(\Phi_B A_{op} \eta q + \overline{j_D} A_{st}\right) \tau_i \qquad (7-4)$$

which, therefore, defines the saturation signal charge for a given background, dark current, and integration time. The corresponding signal voltage is then:

$$V_{sig} = \frac{Q_{sig}}{C_N} \bullet g \qquad (7-5)$$

where C_N is the output node capacitance and g is the processor gain.

Equation (7-4) predicts that the maximum CIM output signal decreases linearly with integration time τ_i, in agreement with the data of Figure 7-14: the observed saturation level decreases in equal increments from $\tau = 6$ μs, to 8 μs, to 10 μs. (Extrapolating these points, saturation for $\tau = 4$ μs should occur at a signal level of ~675 mV.) Similarly, the slope of the response curve for small signal flux increases with τ as predicted, but (as for the 65 K case) is not strictly proportional to τ. This discrepancy is not understood.

The performance of 8B-081 at T = 80 K was unexpected in light of the MIS screening results at this temperature (Section VII.B), which indicated inadequate MIS dark storage times on the CIM rows. It is possible that the actual device temperature during 80 K screening was several degrees higher than assumed, since the temperature was carefully monitored only during initial cooldown to 65 K. For subsequent 80 K testing, the nitrogen reservoir was restored rapidly to atmosphere and time allowed for the device to equilibrate; if the temperature rise was sufficiently rapid, the thermal seal between the dewar coldfinger and device tub could fail, resulting in a higher operating temperature and degraded MIS performance.

Uniformity of response at 66 K is illustrated in Figure 7-15 for 27 randomly selected elements of one detector row. Integration time was 8 μs and signal flux approximately $9 \times 10^{15}/cm^2s$. The mean signal voltage (output referred) was 317 mV with a standard deviation of 47 mV uncorrected, and none of the sampled outputs was nonresponsive. Corresponding mean responsivity was 107 MV/W (output referred). For these measurements, the CIM operating parameters (detector row bias, diode reverse bias, etc.) were optimized for an average pixel of the given row and were not readjusted for each pixel measured.

Figure 7-16 shows similar data for randomly selected elements of three detector rows at 66 K and 4-μs integration subject to the same signal flux. Pixels of rows 2 and 4 coupled to the same diode column have output signals that track fairly closely, while the pixels of row 10 (on the other half of the array), coupled to a different set of diode columns, show no correlation with the output signals of these two rows. These limited data suggest that variation in diode character may be the principal factor limiting uniformity of response in this array. If this is the case, a 100°C postanneal could be expected to improve signal uniformity by reducing diode leakage currents to levels at which variations in leakage produce no significant variations in CIM output signal. Since 8B-081 was the designated contract deliverable, however, postanneal was not performed before delivery.

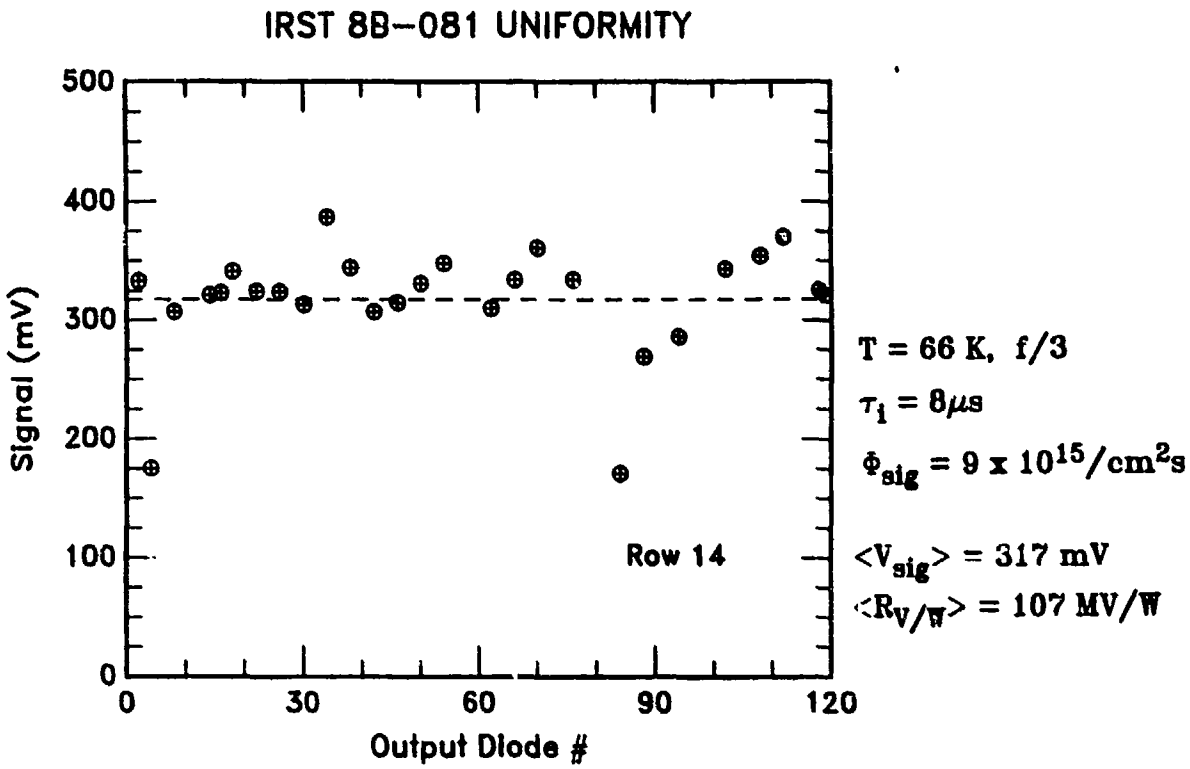


Figure 7-15. Response uniformity data for randomly selected elements of one row of IRST 8B-081 at T = 66 K and 8-μs integration time. Mean responsivity was 107 MV/W (output referred).

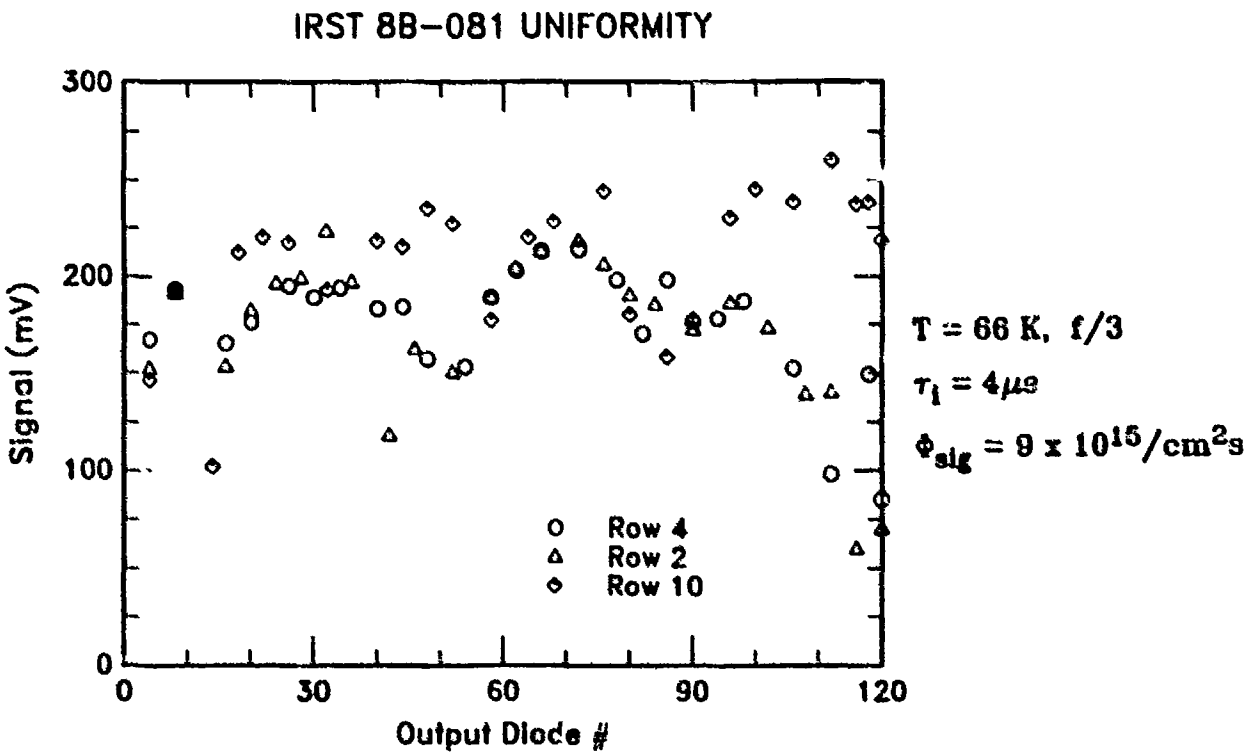


Figure 7-16. Response uniformity data for randomly selected elements of three rows of IRST 8B-081 at T = 66 K and 4-μs integration time. Two rows (2 and 4) are on same side of CIM array; third row is on opposite side and couples to different set of output diodes.

The average responsivity obtained from Figure 7-15 can be compared with the predicted responsivity, obtained by substituting for V_{sig} in Equation (7-1) the predicted CIM output signal voltage given by:

$$V_{sig} = g \bullet \frac{Q_{sig}}{C_N} = \frac{g}{C_N}\left(\Phi_{sig} A_{op} \eta q \tau_i\right)$$

Substitution gives

$$R_{V/W} = \frac{\eta q \tau_i g}{C_N} \bullet \frac{\lambda_p}{hc}$$

For a quantum efficiency of 0.5, an estimated node capacitance of 5 pF, and a (measured) processor gain of 10, the predicted responsivity at the CIM output for $\tau_i = 8$ μs is 64 MV/W, about 40% smaller than the measured mean value.

This discrepancy can be only partially reconciled by assuming a slightly higher quantum efficiency ($\eta > 60\%$ is unrealistic for thin-nickel gates) or slightly lower node capacitance (values < 5 pF have not been observed for a CIM output wire-bonded to an external processor). It is possible that a source of extraneous signal is somehow contributing to the total charge sensed by the diode output during charge transfer. A likely candidate is the narrow transparent region around the contact window at the termination of each diode column, which admits IR signal directly onto a small area of active diode that can itself act as a detector, and that has a total area nearly half the pixel active area. A high-resolution IR spot scan would be required to answer this question, and this was not performed on 8B-081 before delivery. Subsequent photomask revisions, however, eliminated the transparent region from the CIM cell design, beginning with the first vertically integrated CIM lot.

Detector noise measurements were also performed on 8B-081 before delivery, and these demonstrated that FPA sensitivity was heavily dominated by excess system noise. Measured values for D* (λ_p) were in the range of high 10^9 cmHz$^{1/2}$/W, at least a factor of 5 lower than the performance prediction, and signal photon noise could not be discriminated from the total noise spectrum. During subsequent VICIM process development, considerable effort was devoted to reducing the noise contribution of the FPA dewar and external electronics, and the result was a much improved, lower-noise test system that is currently in use with the first prototype VICIM arrays.

SECTION VIII
SUMMARY AND CONCLUSIONS

The primary goals of this development program were the design, fabrication, and operation of a 480 × 4 scanning CIM sensor array for 8- to 12-μm IRST applications. Although the ultimate goal of imaging a vertically integrated TDI array in scanning mode was not accomplished during the contract period, a number of key technical milestones were achieved that together comprise the requisite technology demonstration for CIM LWIR scanning-array feasibility. These include:

- Functional demonstration, with row-and-column performance analysis, of bondable prototype arrays of both configurations, fabricated on unthinned HgCdTe substrates and coupled to existing Si IC focal-plane processors. Measured responsivity, linearity, and saturation flux met or exceeded IRST performance goals.
- Implementation of advanced fabrication processes that resulted in significant enhancement of CIM array yields. The most recent lots fabricated under contract funding exhibited average detector row yields in excess of 90 percent, with near-100%-yield of upper-level control gates. In addition, fusible interconnects were effective in isolating more than half the electrical defects in these high-yielding arrays.
- Demonstration of enhanced MIS properties, i.e., reduced dark currents with no type conversion, in thinned p-type HgCdTe substrates, as required for both CIM performance enhancement and VICIM fabrication.
- Design, fabrication, and testing of two custom silicon IC focal-plane processors. Completed ICs met or exceeded all performance specifications, with sufficient fabrication yields to exceed projected VICIM development needs.
- Design, assembly, and testing of a dewar module and electronics test station for full operation of the bonded 480 × 1 linear focal-plane array, and diagnostic evaluation of the 480 × 4 TDI array.
- In the parallel technology study, demonstration of leakage-current reduction for ion-implanted CIM diodes using new stable surface passivations combined with thermal postannealing, and investigation of diode 1/f noise mechanisms. The dramatic reduction in diode leakage will mean significant reduction in associated diode shot noise, which was shown to be a major component of excess CIM detector noise in the early phase of the study. Observed leakage levels on the IRST arrays tested were consistent with system noise-performance goals.

The essential task remaining at the end of the contract period was to integrate these several ingredients in the fabrication and demonstration of the first vertically integrated CIM focal-plane arrays.

Although the CIM Array Technology program was completed before a vertically integrated CIM was demonstrated, Texas Instruments intends to continue development under IR&D funding.

SECTION IX
ACKNOWLEDGMENTS

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SECTION X
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APPENDIX
IRST ARRAY MODELING

A. Introduction and Definitions

In its simplest form, a scanning focal plane consists of one line of detector elements and a moving mirror arrangement, as shown in Figure A-1. At any instant in time, one line of the scanned scene is projected on the focal plane and is being read. The scene is moving as the mirror is rotated, and the linear array detects and reads lines in a sequential manner until the entire scene has been scanned.

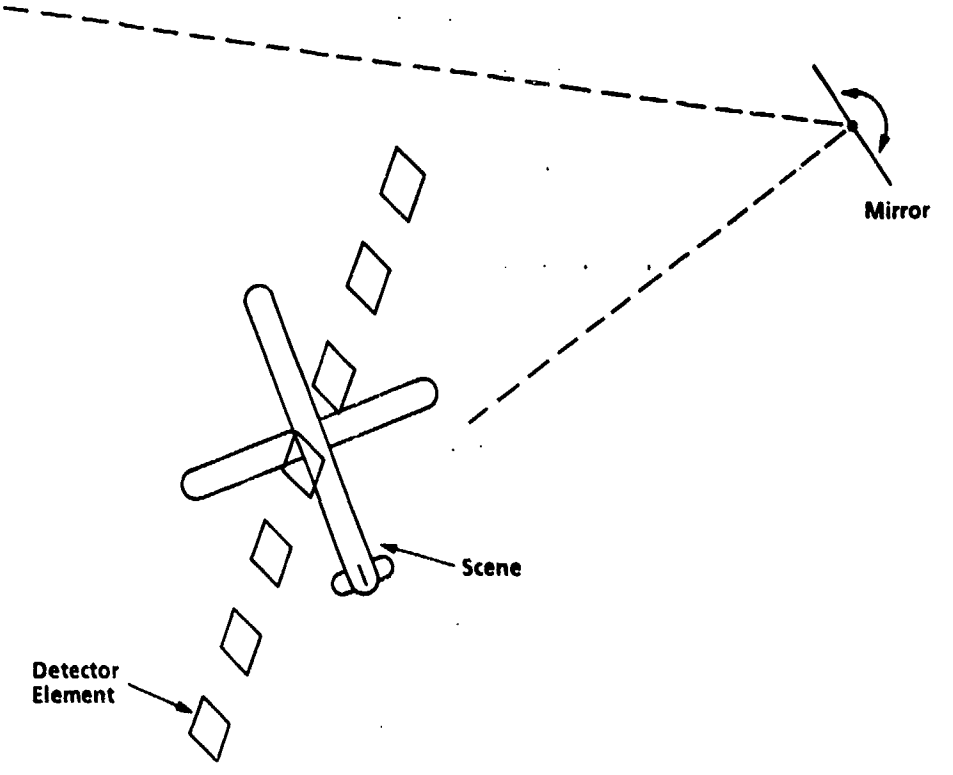

Figure A-1. Mirror-scanned linear array. One line of scene is detected during each dwell period.

The interval of time allowed for the detection of one line is defined as the dwell time. During one dwell, a particular point on the scene will traverse some defined fraction (usually 0.33 to 0.5) of the optically active portion of the detector pixel in the scan direction. During this time period, charge must be integrated and read. For IRST-type systems, the mirror scan rate is very slow, and the dwell time is generally much longer than the available detector integration time. In this situation, the pixel may be integrated and read N times such that:

$$N \bullet (\tau_{int} + \tau_{ct}) \approx N \bullet \tau_{int} = \tau_{dwell} \qquad (A-1)$$

where τ_{int} is the MIS well integration time and τ_{ct} is the time during which charge is being transferred from the MIS well to the diode. The CIM detector is integrating at all times charge is not being transferred, and since τ_{ct} is generally about 100 ns, the duty cycle can be considered to be 100%.

After each integration period, the signal is read into a pixel accumulator; after N such events:

$$V_{sig}(N) = (1-\alpha^N)V_{sig} \qquad (A-2)$$

and

$$V_{noise}(N) = (1-\alpha)\left[\frac{1-\alpha^{2N}}{1-\alpha^2}\right]^{1/2} V_{noise} \qquad (A-3)$$

Here, $V_{sig}(N)$ is the stored signal voltage after pixel accumulation, V_{sig} is the signal voltage at the input to the accumulator, $V_{noise}(N)$ is the stored noise voltage, V_{noise} is the input noise voltage, and α is a property (related to the accumulator capacitance ratio) of the pixel accumulator. After N signals are read into the accumulator, the resultant stored signal is extracted from the focal plane and the accumulator is cleared making it ready for the next dwell period. The use of a pixel accumulator allows the full dwell time to be used (as opposed to a single integration time) and results in a signal-to-noise enhancement given by:

$$\frac{S}{N}(N) = \left[\frac{(1+\alpha)(1-\alpha^N)}{(1-\alpha)(1+\alpha^N)}\right]^{1/2} \bullet \frac{S}{N} \qquad (A-4)$$

where S/N(N) is the signal-to-noise ratio after N integrations per dwell.

Further signal-to-noise enhancement can be achieved using the time delay and integrate (TDI) technique. In this situation, the array has M rows, each of which at any one time is reading a separate line of the scene. After an appropriate time delay, the line read by row 1 is read again by row 2, and this information is added together (on a pixel accumulator or box-car integrator), as shown schematically in Figure A-2. Each scene line is read a total of M times for a total signal-to-noise enhancement (assuming a pixel accumulator addition) of:

$$\frac{S}{N}(N,M) = \left[\frac{(1+\alpha)(1-\alpha^N)}{(1-\alpha)(1+\alpha^N)}\right]^{1/2}\left[\frac{(1+\alpha)(1-\alpha^M)}{(1-\alpha)(1+\alpha^M)}\right]^{1/2} \bullet \frac{S}{N} \qquad (A-5)$$

S/N is the signal-to-noise ratio after one pixel integration period and S/N(N,M) is the signal-to-noise ratio after N integrations per dwell and M time delay and integrates.

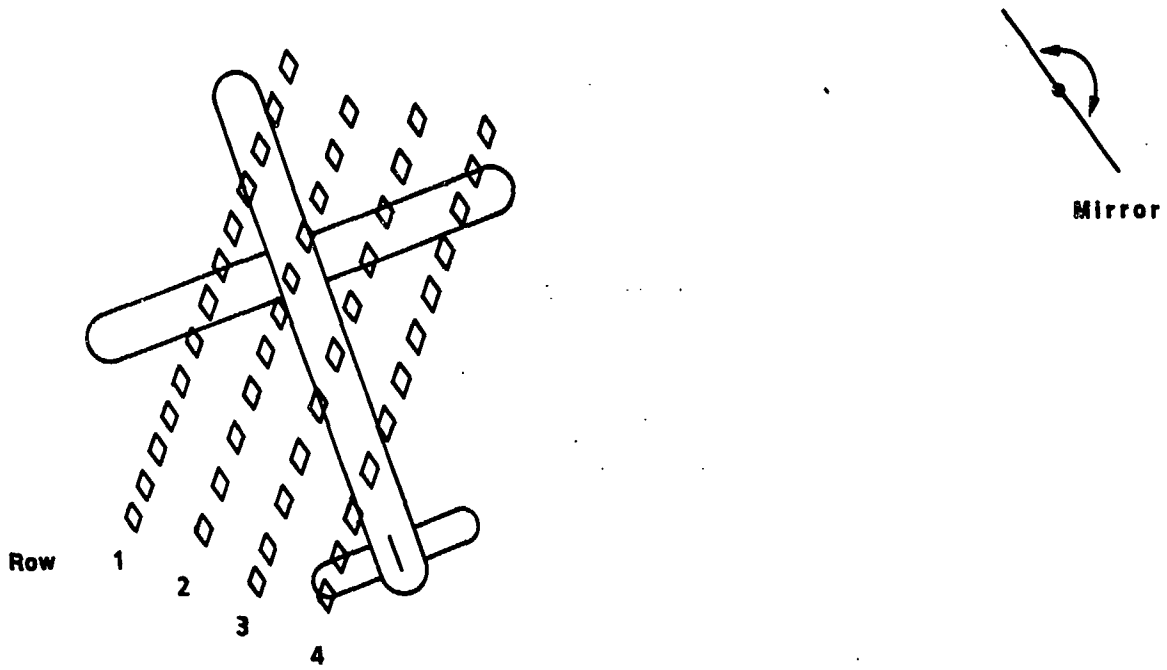

Figure A-2. Four-TDI scanned linear array. At instant in time shown, four lines of the scene are being detected with information going to four pixel accumulators. During each full scan of the scene (one frame), each line will be detected (and added to some memory location) four times.

B. CIM Detector

For a CIM detector, the output signal after N integrations per dwell and M TDIs is:

$$V_{sig}(N,M) = \left(1-\alpha^{N}\right)\left(1-\alpha^{M}\right)\frac{q\Phi_{sig}\eta A_{opt}\tau}{C_N} \qquad (A-6)$$

Where τ is the MIS integration time, A_{opt} is the pixel optical area, η is the optical-area quantum efficiency, Φ_{sig} is the signal flux, C_N is the sense-node capacitance, and q is the charge of an electron. The rms output noise (assuming that the pixel accumulator contributes no noise) is given by:

$$V_{rms}(N,M) = (1-\alpha)\left[\frac{\left(1-\alpha^{2N}\right)}{\left(1-\alpha^{2}\right)}\right]^{1/2}(1-\alpha)\left[\frac{\left(1-\alpha^{2M}\right)}{\left(1-\alpha^{2}\right)}\right]^{1/2}\left[A_{opt}\tau\left(\eta\Phi_{B}+\frac{KJ_d}{q}\right)+\frac{V_{proc}^2C_N^2}{q^2}+\frac{V_d^2C_N^2}{q^2}\right]^{1/2} \qquad (A-7)$$

where Φ_B is the background flux density, J_d is the MIS well dark-current density, K is the ratio of MIS storage to optically active area, V_{proc} is the processor rms noise (per read operation after correlated double sampling), and V_d is the rms noise from the diode (also per read after correlated double sampling).

C. Noise-Equivalent Temperature Difference

The change in scene temperature (above or below some background level) required to give a signal-to-noise ratio of 1 is called the noise-equivalent temperature difference (NEΔT) and is a

standard figure of merit for an IR detector. This is a direct measure of the sensitivity of a system with fixed optics (and flux levels) and allows optimization of the signal-to-noise ratio as a function of the system operating and design parameters (processor bandwidth, number of pixel accumulates, ratio of pixel storage to optical area, etc.).

For a CIM detector operating with N integrations per dwell and MTDIs, NEΔT is given by:

$$\Delta T(N,M)=\left[\frac{(1-\alpha)(1+\alpha^{N})}{(1+\alpha)(1-\alpha^{N})}\right]^{1/2}\left[\frac{(1-\alpha)(1+\alpha^{M})}{(1+\alpha)(1-\alpha^{M})}\right]^{1/2}\frac{\left[A_{opt}\tau\left(\eta\Phi_{B}+\frac{KJ_{d}}{q}\right)+\frac{V_{proc}^{2}C_{N}^{2}}{q^{2}}+\frac{V_{d}^{2}C_{N}^{2}}{q^{2}}\right]^{1/2}}{A_{opt}\eta\tau\Phi_{1}} \qquad (A-8)$$

where Φ_1 is the system signal flux for a 1° change in scene temperature (a function of optics speed, optics transmission, etc.). It has also been assumed that both pixel accumulators have the same value for α.

A Fortran program was written to calculate NEΔT for sensitivity optimization of an IRST system. The program calculates the NEΔT after integration, N integrations per dwell, and M time delay and integrations, and indicates in the output if the MIS well or diode capacity has been exceeded.

D. Figures of Merit

The imaging demonstration of a linear CIM array will use an existing test system built for an IRST program. This system has a dwell time of 48 μs and the information from six sequential dwell periods is averaged with a box-car integrator. The information for each pixel of the imaged scene is read from the focal plane after the six averages, as shown in block diagram form in Figure A-3. From a signal-to-noise standpoint, the sequential averaging is equivalent to six TDIs.

If the pixel is integrated N times per dwell, the NEΔT is given by:

$$\Delta T=\frac{1}{\sqrt{M}}\left[\frac{(1-\alpha)(1+\alpha^{N})}{(1+\alpha)(1-\alpha^{N})}\right]^{1/2}\frac{N_{RMS}}{A_{opt}\eta\tau\Phi_{1}} \qquad (A-9)$$

Here, N is the number of integrations per dwell, M is the number of sequential averages, α is a property of the pixel accumulator circuit (a capacitance ratio, generally 0.6 to 0.8), and N_{RMS} is the rms number of detector noise electrons per integration period. N_{RMS} is given by:

$$N_{RMS}=\left[A_{opt}\tau\left(\eta\Phi_{B}+\frac{J_{d}K}{q}\right)+\frac{I_{d}\tau_{r}}{q}+\frac{C_{N}^{2}V_{p}^{2}}{q^{2}}\right]^{1/2} \qquad (A-10)$$

as in the last term of Equation (A-8), with the diode contribution expressed in terms of the leakage current, I_d, and the clamp-to-sample time, τ_r, of the correlated double sampler.

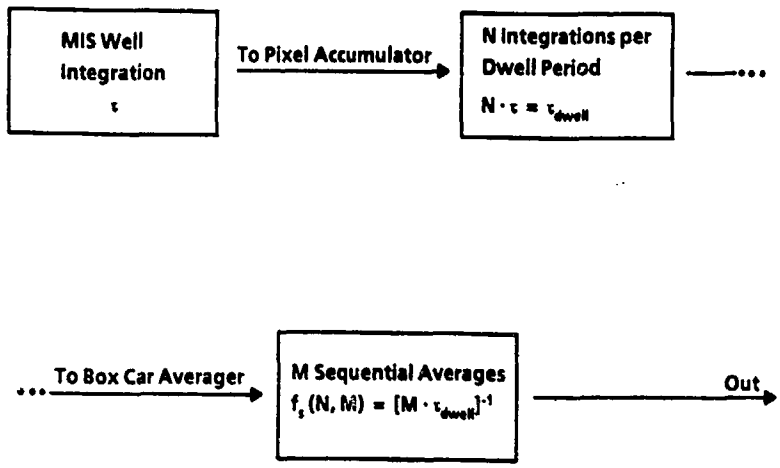

Figure A-3. Data flow for IRST test system with sequential averaging.

Detectivity, D_λ^* (N,M), at wavelength λ is calculated at the point in the signal chain where the information is taken from the focal plane (after N integrations per dwell and M sequential averages). For the IRST test system, the signal is sampled at intervals of $\tau_{out} = M \bullet \tau_{dwell} = [f_S(N,M)]^{-1}$ and the aliased noise-voltage spectral density is given by:

$$v(N,M) = V_{NOISE}(N,M)\left(\frac{2}{f_s(N,M)}\right)^{1/2} \qquad (A-11)$$

In this expression, $V_{NOISE}(N,M)$ is the rms detector noise voltage after N integrations per dwell and M sequential averages and v(N,M) is the corresponding noise voltage density.

The detectivity is given by

$$D_\lambda^*(N,M) = \sqrt{M}\left[\frac{(1+\alpha)(1-\alpha)^N}{(1-\alpha)(1+\alpha)^N}\right]^{1/2} \frac{\lambda}{hc} \frac{\eta\tau A_{opt}^{1/2}}{N_{RMS}} \left(\frac{f_s(N,M)}{2}\right)^{1/2} \qquad (A-12)$$

where h is Planck's constant and c is the speed of light.

E. Signal-Processing Considerations

Efficient on-detector multiplexing during operation of a CIM detector in a scanned system demands that the total time spent to read each pixel (this includes resetting the diode, the CDS clamp operation, charge transfer, and the sample operation) be minimized. For a TDI array, all read operations must be accomplished within the dwell period as expressed by:

$$\tau_{read} \bullet N \bullet M \bullet P \leq \tau_{dwell} \qquad (A-13)$$

Here, N•M•P (where P is the number of TDI "strings" that are read by each diode) is the number of times the diode is read during one dwell period and τ_{read} is the total time for each read operation. For a non-TDI array (such as when sequential averaging is used), M = 1.

During the read operation, the processor preamplifier must respond to the diode change in bias within the CDS clamp-to-sample time. If the processor preamplifier bandwidth rolls off as a single-pole filter with B as the –3-dB point, adequate amplifier response requires a lower limit of the product of B and τ_r of about 1, i.e.:

$$\tau_r \bullet B \geq 1 \qquad (A-14)$$

Finally, since the dwell time is generally much longer than the available MIS integration time, each pixel can be read N times during each dwell period, or:

$$\tau \bullet N \leq \tau_{dwell} \qquad (A-15)$$

The available integration time is given by:

$$\tau = \frac{(V_g - V_{th})C_{MIS}}{\frac{q\Phi_{MAX}\eta}{K} + J_d} \qquad (A-16)$$

where C_{MIS} is the MIS gate insulator capacitance, Φ_{MAX} is the maximum incident flux level, V_{th} is the MIS gate threshold voltage, and V_g is the maximum gate bias (at the onset of MIS well tunnel breakdown).

F. System and MIS Well Characteristics

System optics, segment of the IR band, flux levels, and dwell time for the initial imaging demonstration were determined by an existing IRST focal plane program at Texas Instruments. Performance calculations for cutoff wavelengths of 9.5, 10.5, and 11.3 μm were completed using the flux levels shown in Table A-1. The 1° signal flux levels were determined assuming *f*/2.5 optics with 60% transmission. The pixel optically active area was taken to be 2.72 mil^2.

Table A-1. Performance Calculation

Material Cutoff (μm)	9.5	10.5	11.3
Minimum Flux (ph/s–cm ^{2})	4×10^{15}	7×10^{15}	1×10^{16}
Maximum Flux (ph/s–cm ^{2})	2×10^{16}	4×10^{16}	5×10^{16}
1° Signal Flux	1.0×10^{14}	1.6×10^{14}	2.0×10^{14}

MIS dark-current density (nontunneling) was calculated assuming the use of thinned material (which can reduce bulk diffusion dark-current density by a factor of 10). If the minority carrier lifetime is taken to be 1 μs, the mobility to be 50,000 cm^2/V-s, the acceptor density to be 8×10^{14} cm^{-3}, and the substrate temperature to be 79 K, the calculated dark-current densities are given by

Table A-2. The total MIS dark-current density was calculated by adding the depletion region dark current and 10% of the bulk diffusion dark-current density.

Table A-2. Calculated MIS Dark-Current Densities

Material Cutoff (μm)	9.5	10.5	11.3
Diffusion Dark-Current Density (A/cm^2)	9.5×10^{-5}	5.1×10^{-4}	1.6×10^{-3}
Depletion Dark-Current Density (A/cm^2)	4.8×10^{-5}	9.4×10^{-5}	1.5×10^{-4}
Total Dark-Current Density (A/cm^2)	6×10^{-5}	1.4×10^{-4}	3.1×10^{-4}

The maximum MIS well capacity is generally defined to occur at that gate bias past threshold where the empty-well tunnel-breakdown-generated dark current is equal to the optically generated current.The tunnel-current dependence on gate bias is exponential and can be thought of as an on-or-off phenomenon. Using an acceptor concentration of 8×10^{14} cm^{-3} and Shockley-Read center density (midgap states) of 1×10^{13} cm^{-3}, the maximum empty-well depletion region electric fields were calculated for each material bandgap from:

$$J_{tun} = q\Phi_{MIN}\eta \cdot \frac{1}{2} \qquad (A-17)$$

The quantum efficiency was taken to be 0.5 and the factor of 2 was added since, in general, the MIS storage area will be greater than the optically active area for scanned systems. A simple depletion model was then employed to calculate the maximum gate bias, assuming an MIS insulator capacitance of 4×10^{-8} F/cm^2. The product of the gate bias past threshold and the insulator capacitance is then the well capacity. The results of these calculations are shown in Table A-3.

Table A-3. MIS Well Capacity

Material Cutoff (μm)	9.5	10.5	11.3
Tunnel Breakdown Field (V/μm)	0.95	0.80	0.72
Maximum Bias Past Threshold (V)	0.74	0.54	0.45
Well Capacity ($coul/cm^2$)	2.9×10^{-8}	2.1×10^{-8}	1.8×10^{-8}

G. Performance Calculations

Both TDI and non-TDI (using sequential averaging) arrays will be designed and fabricated. The non-TDI arrays will employ four rows for both oversampling in the spatial domain and array redundancy. If adjacent columns of MIS wells are read by the same diode, the number of pixels read by each diode will be four (see Figure 2-9). Pixel-to-pixel spacing in the cross-scan direction is 3 mils, and the pitch in the scan direction is 6 mils.

The optimum pixel architecture is determined by calculating D_λ^* (N,M) or NEΔT as a function of the ratio of MIS storage area to optically active area. The use of through-the-material (via) type interconnects (with thinned material) to the processor circuit allows for very low node capacitances, and the minimum node capacitance needed to hold the transferred MIS well charge was used in the calculations. A diode bias swing of 0.2 V was assumed for node capacitance calculations. Calculations were performed for diode leakage currents of 5.0 mA/cm^2 and 0.0 mA/cm^2 (insignificant diode noise) with a diode area of 5.2 mil^2. [At 5.0 mA/cm^2, the diode contribution to noise (per read operation) is 723 electrons. This is comparable to actual measurements made on unbaked diodes where the total noise (both shot and 1/f) was about 1,000 electrons.] Unless otherwise noted, the MIS dark-current densities, well capacitances, and flux levels from Tables A-1 through A-3 were used. Calculations were performed for thinned-nickel (optical area quantum efficiency of 0.5) transparent gates and for open-window structures (quantum efficiency of 0.8).

The silicon processor bandwidth was taken to be 2 MHz for all calculations with a clamp-to-sample time of 0.5 μs. The processor noise voltage density (white, before correlated double sampling) was 5 nV/Hz$^{1/2}$, which gives an after-CDS rms noise voltage of 10 μV for this bandwidth and clamp-to-sample time. The use of high bandwidth and short clamp-to-sample time keeps diode shot noise to a minimum. The α value for the pixel accumulator circuit was taken to be 0.7, and the number of sequential averages was six for all calculations. For detectivity calculations, λ was taken to be the material cutoff wavelength.

Calculations for 10.5-μm material with thin nickel gates are tabulated in Table A-4, which illustrates the logic used for each set of calculations. For each value of K (storage-to-optical-area ratio), the maximum integration time is calculated that determines the number of integrations per dwell (N). In each case, the integration time used is slightly less than the maximum available time, to give $\tau \cdot N = \tau_{dwell}$. Thus, almost 100% of the available dwell time is used for MIS integration of charge. The node capacitance needed to accommodate the MIS well charge is calculated, and NEΔT and D_λ^* (N,M) are calculated for two diode dark-current densities.

The results of Table A-4 are plotted in Figure A-4. In the zero diode dark-current case, the optimum value of K is very low since the contribution from the MIS well dominates the device noise and peak performance is obtained with a small MIS dark-current shot-noise contribution. At the higher diode dark-current density, the optimum K value is higher, since the higher noise contribution per read operation (from the diode) tends to favor situations with lower integrations per dwell period. Similar calculations for 9.5-μm material and 11.3-μm material are shown in Figures A-5 and A-6.

Table A-4. NEΔT and D_λ^* (N, M) for 10.5-μm Detectors With Thin Nickel Gates

K	τ (μs)	N	C_{node} (pF)	J_{diode} (mA/cm²)	NEΔT (K)	D_λ^* (N,M) (×10¹¹ cm-Hz^½/W)
1.1	6.82	7	1.9	0.0	0.0148	2.225
1.4	9.55	5	2.6	0.0	0.0141	2.34
1.8	11.93	4	3.4	0.0	0.141	2.33
2.5	15.91	3	4.6	0.0	0.0145	2.27
4.0	23.87	2	7.3	0.0	0.0159	2.08
1.1	6.82	7	1.9	5.0	0.0204	1.61
1.4	9.55	5	2.6	5.0	0.0179	1.85
1.8	11.93	4	3.4	5.0	0.0170	1.94
2.5	15.91	3	4.6	5.0	0.0166	1.99
4.0	23.87	2	7.3	5.0	0.0171	1.93

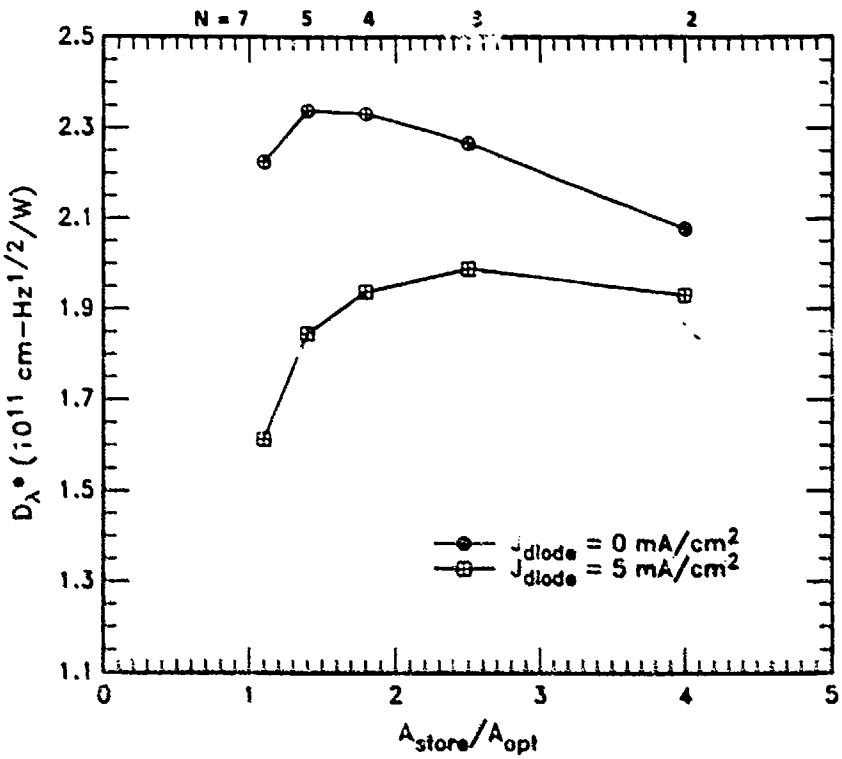

Figure A-4. Detectivity as function of ratio of MIS storage area to optically active area (K) for 10.5-μm IRST detector. Quantum efficiency was 0.5.

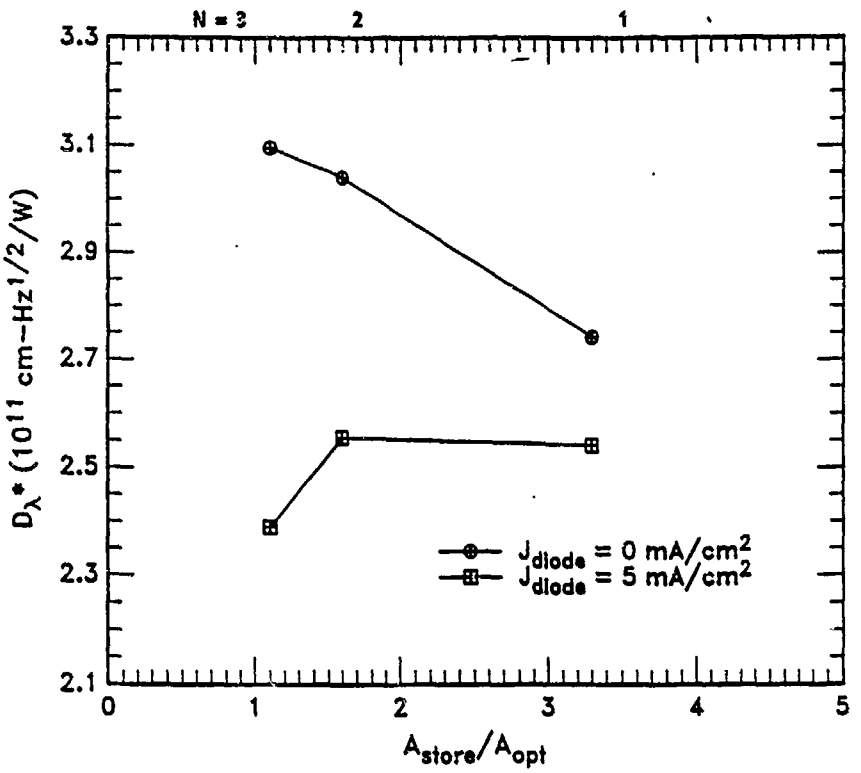

Figure A-5. Detectivity versus K for 9.5-μm IRST detector. Quantum efficiency was 0.5.

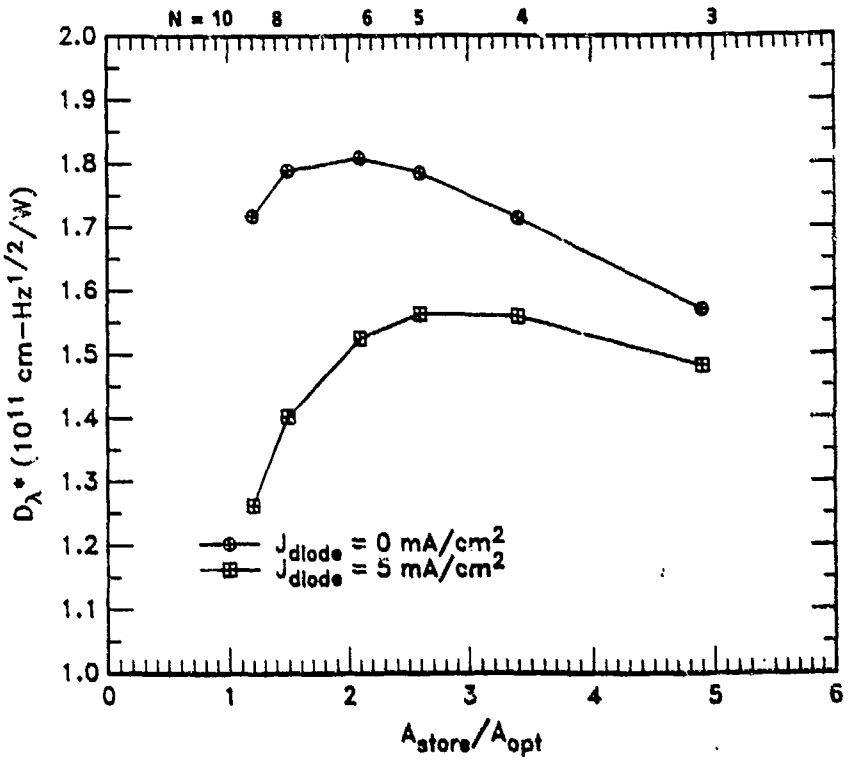

Figure A-6. Detectivity versus K for 11.3-μm IRST detector. Quantum efficiency was 0.5.

Performance is good with $D\lambda^*$ varying from 1.5 to 3.0×10^{11} cm-Hz$^{1/2}$/W and NEΔTs from 0.02 to 0.015 K, depending on material cutoff and diode dark-current density. Figures A-7 and A-8 compare performance for detectors with different material cutoffs. Figure A-9 shows the degradation of performance with increasing MIS dark-current density for 11.3-μm detectors. The figures show that architectures with smaller storage-to-optical area ratios are somewhat less susceptible to this type of degradation.

H. Open-Window Detectors

Significant gains in optical-area quantum efficiency can be achieved by using open-window pixel architectures, as discussed in Subsection II.C. In this architecture, the long diffusion lengths of optically generated minority carriers are used to collect carriers from nongate-controlled or "open" areas. Quantum efficiencies as high as 80% on n-type devices have been achieved using this concept.

A comparison of performance for open-window and thinned-nickel gates is shown in Figures A-10 through A-12. Calculations show performance levels as high as 3.9×10^{11} cm-Hz$^{1/2}$/W with an NEΔT of 0.012 K. Figure A-13 compares open-window performance for different detector cutoffs.

I. Conclusions

Several design decisions can be drawn from the IRST modeling study. Figures A-7, A-8, and A-13 show that the optimum storage-to-optical-area ratio varies from 1 to 3 with material cutoff, diode leakage current density, and quantum efficiency. Since lower ratios are less susceptible to performance degradation caused by increases in MIS dark-current density, a value of K between 1.5 and 2 was selected. Designs with minimum diode area were employed to keep the diode noise per read operation to a minimum. Because of MIS dark-current densities and processor noise levels, detector performance increases faster than the 1/2 power with increases in quantum efficiency. Open-window design options were included in the array to take advantage of this situation.

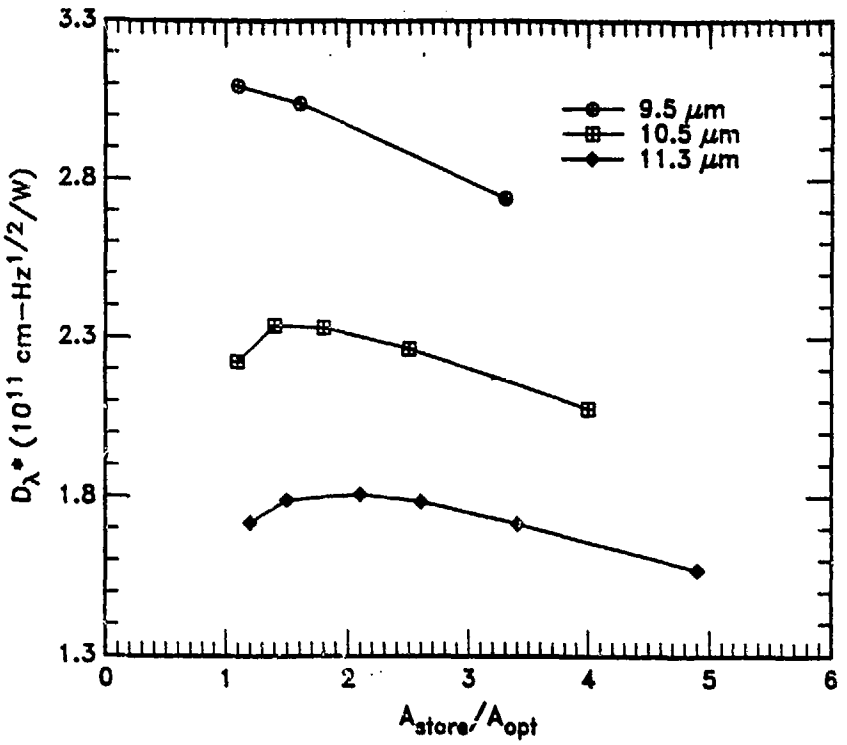

Figure A-7. Detectivity versus K compared for 9.5-, 10.5-, and 11.3-μm IRST detectors. Diode leakage current was taken to be zero. Quantum efficiency was 0.5.

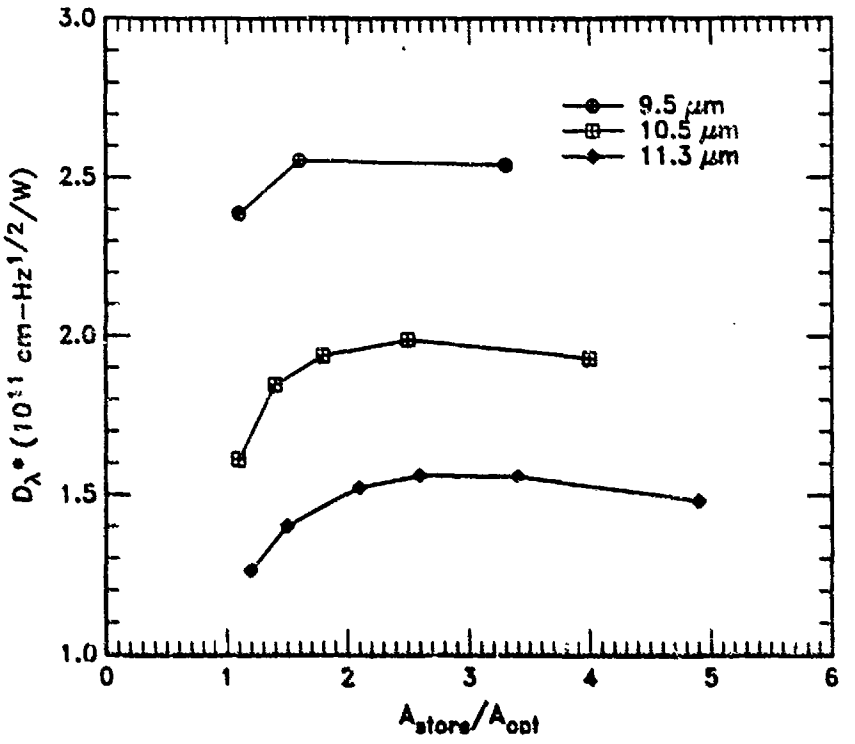

Figure A-8. Detectivity versus K compared for 9.5-, 10.5-, and 11.3-μm IRST detectors. Diode leakage current was 5 mA/cm^2. Quantum efficiency was 0.5.

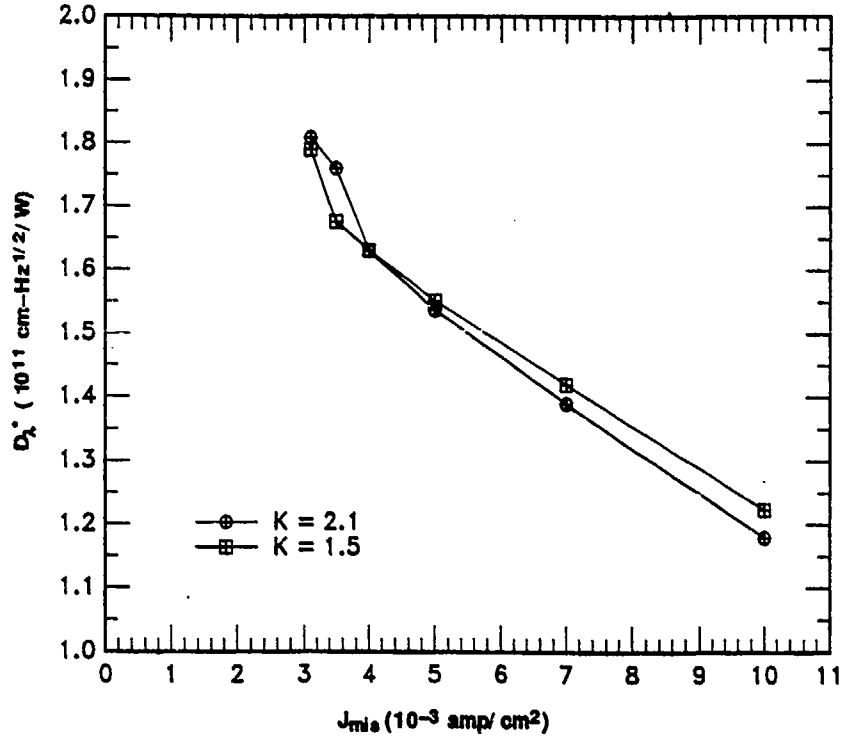

Figure A-9. Detectivity versus MIS dark-current density for 11.3-μm IRST detector. Circles are for K = 2.1 and squares for K = 1.5. Quantum efficiency was 0.5.

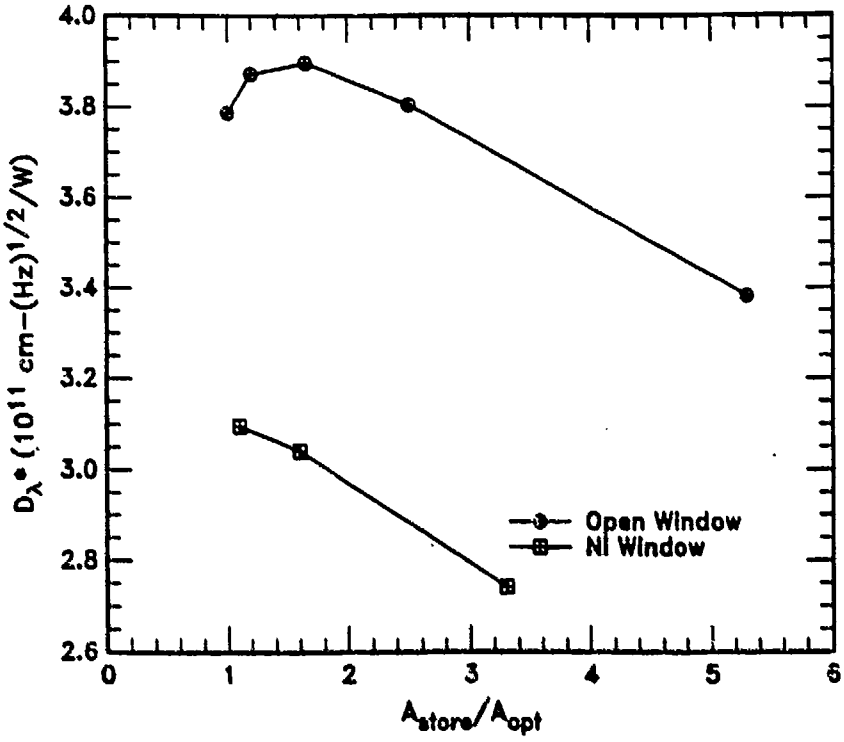

Figure A-10. Detectivity versus K for open and thinned-nickel window 9.5-μm IRST detectors. Ni window quantum efficiency was 0.5 and open-window QE was 0.8.

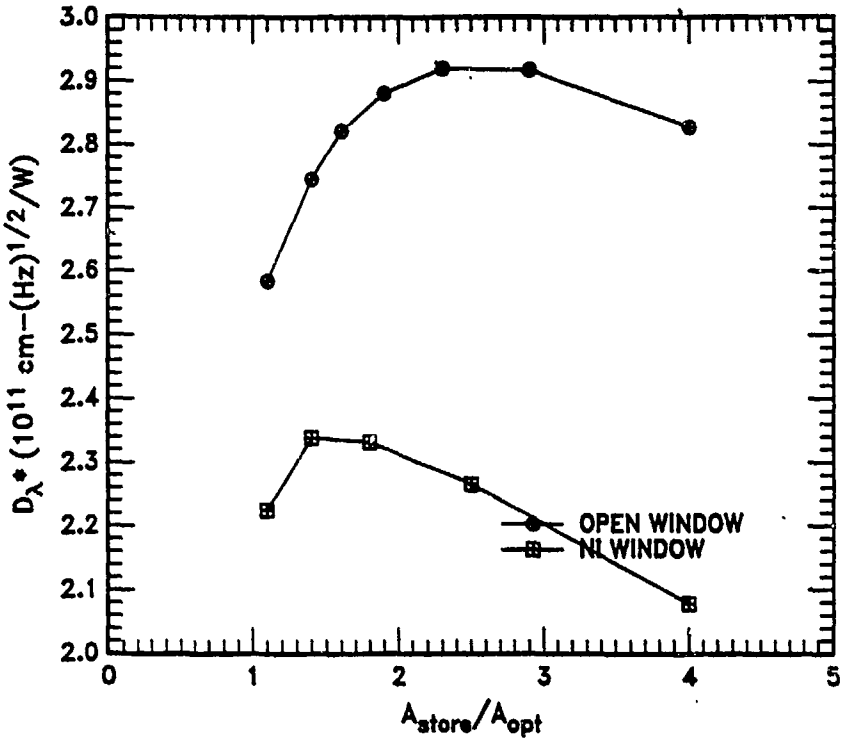

Figure A-11. Detectivity versus K for open and thinned-nickel window 10.5-μm IRST detectors. Ni window quantum efficiency was 0.5 and open-window QE was 0.8.

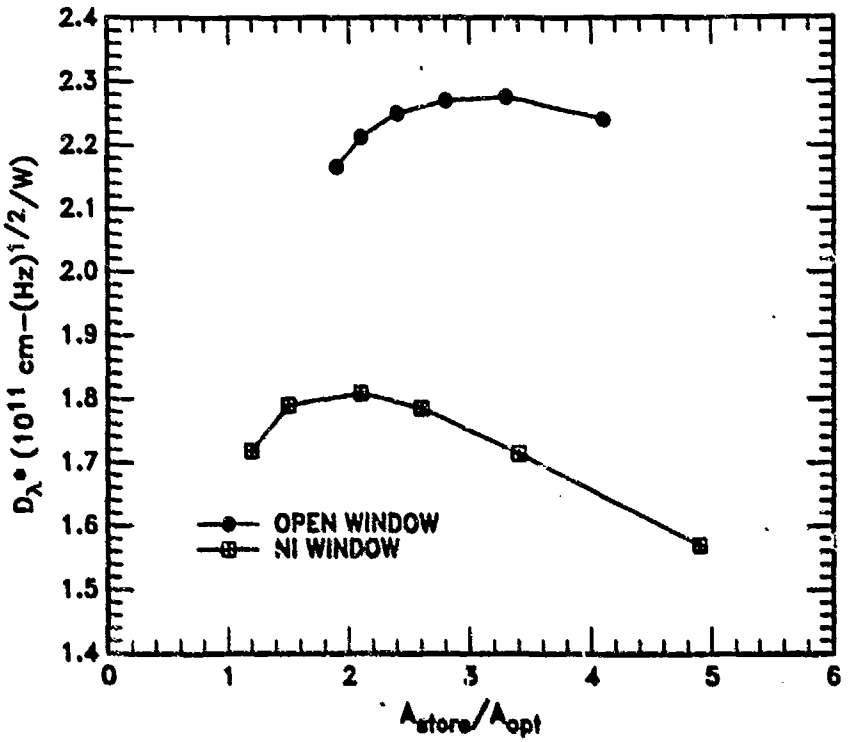

Figure A-12. Detectivity versus K for open and thinned-nickel window 11.3-μm IRST detectors. Ni window quantum efficiency was 0.5 and open-window QE was 0.8.

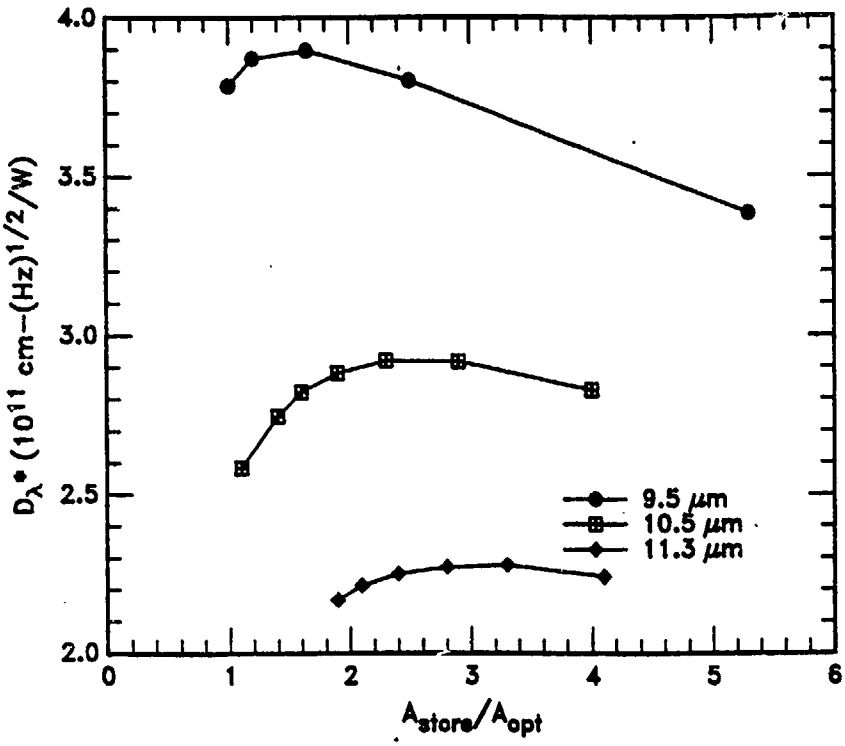

Figure A-13. **Detectivity versus K compared for 9.5-, 10.5-, and 11.3-μm open-window IRST detectors. Quantum efficiency was 0.8.**